# VX4730
# 12-Channel D/A Module
# Operating Manual

Tektronix

11/11/92 9201-01-A

## WARRANTY

This Tektronix, Inc. product is warranted against defects in materials and workmanship, and is warranted to meet the performance specifications as listed in the current catalog and/or data sheet for this product. This warranty applies for **three (3) years** following the date of shipment. Tektronix will, at its option, repair or replace, at no cost to the customer, this product should it prove to be defective during the warranty period, provided the defect or failure is not due to misuse or abuse of the product. The customer is responsible for shipment of the defective product to the Tektronix repair facility. NO OTHER WARRANTY IS EXPRESSED OR IMPLIED, INCLUDING WARRANTY FOR FITNESS OF PURPOSE. TEKTRONIX INC. SHALL, IN NO CASE, BE LIABLE FOR CONSEQUENTIAL DAMAGES.

## TRADEMARK NOTIFICATION

Printed in U.S.A.

# Operators Safety Summary

The general safety information in this summary is for both operating and servicing personnel. Additional specific warnings and cautions are found throughout the manual where they apply, and may not appear in this summary.

## TERMS

### In This Manual

**WARNING** statements identify conditions or practices that could result in personal injury or loss of life.

**CAUTION** statements identify conditions or practices that could result in damage to the module or other property.

### Marked on the Module

**DANGER** indicates a personal injury hazard immediately accessible as one reads the marking.

**CAUTION** indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property, including the module itself.

## SYMBOLS

### In This Manual

⚠ This symbol indicates where applicable cautionary or other information is to be found.

ⓘ This symbol indicates where special explanatory information is included in the manual. There is no caution or danger associated with the information.

### Marked on the Module

ϟ **DANGER** — High Voltage.

⏚ Protective ground (earth) terminal.

⚠ ATTENTION — Refer to the manual.

ⓘ Refer to manual before using.

## Power Source

This module is intended to operate in a mainframe whose power source does not apply more than 250V rms between the supply conductors or between either supply conductor and ground. A protective ground connection through the grounding conductor in the power cord(s) is essential for safe operation.

## Grounding the Module

This module is grounded through the grounding conductor of the mainframe power cord(s). To avoid electrical shock, plug the mainframe power cord(s) into a properly wired receptacle before connecting to the module connectors. A protective ground connection through the mainframe is essential for safe operation.

## Danger Arising from Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts can render an electric shock.

## Use the Proper Fuse

To avoid fire hazard, use only fuses specified in the module parts list. A replacement fuse must meet the type, voltage rating, and current rating specifications required for the fuse that it replaces.

## Do Not Operate in Explosive Atmosphere

To avoid explosion, do not operate the module in an explosive atmosphere.

## Do Not Remove Covers or Panels

To avoid personal injury, the module covers should be removed only by qualified service personnel. Do not operate the module without covers and panels properly installed.

GOSUB n  Runs the subroutine beginning with line n.  The end of the subroutine is delineated with a RETURN statement.  When the subroutine reaches the RETURN statement, execution will resume on the line following the GOSUB command.

GOTO n  Program branches to line n.

IF/THEN  Sets up a conditional IF/THEN statement.  Used with other commands, so that IF the stated condition is met, THEN the command following is effective.

REM  All characters following the REM command are not executed.

RETURN  Ends a subroutine and returns operation to the line after the last executed GOSUB command.

<CR>  Carriage return character, decimal 13.

<LF>  Line feed character, decimal 10.

# VX4730 MODULE
# QUICK REFERENCE GUIDE

Numbers in parentheses refer to the page(s) in the Operating Manual.

## SETUP

Be sure all switches are correctly set. (p. 1 - 5)
Follow Installation guidelines. (p. 2 - 1)

The default condition of the VX4730 Module after the completion of power-up self test is as follows:

| | |
|---|---|
| Isolation: | Open |
| D/A Output: | 0.000V |
| Input Mode: | Non-buffered |
| Interrupts: | Disabled |

## LEDs

When lit, the LEDs indicate the following:

| | |
|---|---|
| Power | power supplies functioning |
| Failed | module failure |
| Error | an error has been found in self test or programming |
| Message | module is processing a VMEbus cycle |
| CH A - CH L | their respective channel has been programmed since the last reset or CLR command, <u>and</u> their associated isolation relay is closed. |

## SYSTEM COMMANDS

These non-data commands are initiated by the VX4730's commander.  The following VXIbus Instrument Protocol commands will affect the VX4730:

ABORT NORMAL OPERATION
ASYNCHRONOUS MODE CONTROL
BYTE AVAILABLE
BYTE REQUEST
CLEAR
CLEAR LOCK
CONTROL EVENT
END NORMAL OPERATION
ERROR QUERY
IDENTIFY COMMANDER
READ INTERRUPTER LINE
READ INTERRUPTERS
READ PROTOCOL
READ STATUS
RESPONSE ENABLE
SET LOCK
TRIGGER

**COMMAND SYNTAX** Command protocol and syntax for the VX4730 Module is as follows: (3 - 3)

1) If a character is not enclosed by brackets, that character itself is sent, otherwise:
   [] encloses the symbol for the actual argument.
   <CR> = carriage return; <LF> = line feed.

2) Any character may be sent in either upper or lower case form.

3) Any of the following white space characters:

   00 hex through 09 hex    0B hex through 20 hex

   are allowed in any of the following places: before any comma, semicolon, or <lf>; after any comma; in place of any space character. Any number of white space characters may be used together.

4) Any character may be sent in either upper or lower case form.

5) Any binary argument must be formatted as #0[B1][B2]...
   The "#0" characters are only required at the beginning of the binary string.

**MODULE COMMANDS** All commands must end with a terminator (line feed or semi-colon).

A z (ASCII) or A #0z (binary)
Programs a single output voltage level for all DAC channels simultaneously. (3 - 6)

B $v_1v_2...v_{12}$
Programs the output voltage level of the DAC channels specified in previous V, S, or A commands with binary data. (3 - 8)

BUF Puts the module in buffered mode. (3 - 10)

CLR Clears all channel LEDs. (3 - 11)

CLS $z_1,...,z_n$
Closes the module's output isolation relay(s), connecting the output(s) of one or more DACs to the module's output connectors. (3 - 12)

D $v_1v_2...v_{12}$
Programs the output voltage level of the DAC channels specified in previous V, S, or A commands with ASCII characters. (3 - 13)

DINT Disables Request True interrupt generation. (3 - 14)

ERR? Queries the error status of the module. (3 - 15)

INT Enables Request True interrupt generation. (3 - 19)

IST Initiates the module's internal self test. (3 - 20)

NBUF Puts the module in nonbuffered mode. (3 - 21)

OPN $z_1,...,z_n$
Opens the module's output isolation relay(s), disconnecting the output(s) of one or more DACs from the module's output connectors. (3 - 22)

REV? Returns the VX4730's firmware revision level. (3 - 23)

RST Resets the VX4730 to its power-up state. (3 - 24)

S$z_1z_2...z_{12}$ $v_1,v_2,...,v_{12}$<TM> (ASCII) or S$z_1z_2...z_{12}$ #0$v_1v_2...v_{12}$<TM> (binary)

Programs the output voltage level(s) of the specified DAC channel(s). All outputs change synchronously when the command terminator is parsed. (3 - 25)

V$z_1z_2...z_{12}$ $v_1,v_2,...v_{12}$<TM> (ASCII) or V$z_1z_2...z_{12}$ #0$v_1v_2...v_{12}$ (binary)
Programs the output voltage level of the specified DAC channel(s). Each DAC's output voltage changes as that channel's input is parsed. (3 - 28)

**PROGRAMMING** The programming examples in the manual are written in Microsoft GW BASIC. For programming examples, see page 4 - 2.

CALL ENTER (R$, LENGTH%, ADDRESS%, STATUS%)
Inputs data into the string R$ from the IEEE-488 instrument whose decimal primary address is contained in the variable ADDRESS%. LENGTH% = the number of bytes read from the instrument. STATUS% = '0' if the transfer was successful; '8' if an operating system timeout occurred in the PC. To use the CALL ENTER statement, the string R$ must be set to a string of spaces whose length is greater than or equal to the maximum number of bytes expected from the 73A-332.

CALL SEND (ADDRESS%, WRT$, STATUS%)
Outputs the contents of the string variable WRT$ to the IEEE-488 instrument whose decimal primary address is in the variable ADDRESS%. The variable STATUS% = '0' if the transfer was successful and an '8' if an operating timeout occurred in the PC.

END Terminates the program.

FOR/NEXT Repeats the instructions between the FOR and NEXT statements for a defined number of iterations.

# Table of Contents

## Section 1
## General Information and Specifications

## Section 2
## Preparation For Use

## Section 3
## Operation

## Section 4
## Programming Examples

# List of Illustrations

# VX4730
# 12-Channel D/A Module

## Section 1
## General Information and Specifications

### Introduction

The VX4730 12-Channel D/A Module (digital-to-analog converters: D/A or DAC) is a printed circuit board assembly for use in a mainframe conforming to the VXIbus Specification, such as the VX1400 C size mainframe used in the Tektronix/CDS IAC System. The VX4730 consists of twelve (12) independent single-ended 16-bit DACs, individually programmable from -16.3835 volts to +16.3835 volts in 0.5 millivolt steps. Monotonicity is guaranteed to 14 bits.

Each output channel of the DAC provides a minimum of 60 milliamperes of current, with all channels driven. In addition, any individual channel may provide up to ±16.3835 V into a 40 Ohm load. The total current for all twelve channels cannot exceed 720 milliamperes.

The VX4730 incorporates unique features which improve its speed and operational efficiency when installed in an ATE system. The buffered mode automatically enables Fast Handshake protocol, a special provision of the VXIbus Specification that allows commands and/or data to be sent from the system controller to a module with minimum VXIbus protocol overhead. In this mode, the DAC stores incoming data/commands in an internal buffer that is sequentially processed. Module data processing and buffer loading occur simultaneously.

In non-buffered normal transfer mode, information is processed by the DAC on a byte-by-byte basis as it is received. This feature supports applications where it is important that the VX4730's operation remain synchronous with another event in the ATE system.

A combination of the benefits of both non-buffered mode and Fast Handshake mode can be obtained by sending binary data while in the non-buffered mode. In this case, information is processed a byte at a time, but the DAC automatically switches into Fast Handshake mode during the binary transfer.

The DAC may be programmed either in binary or by using ASCII character strings. When using ASCII, the channels to be programmed are specified first, and then the desired voltage level for each channel is specified in engineering units. (For example, "VAC 10,-2" sets channels A and C to 10.000 and -2.000 volts respectively). The voltage level may be indicated in any valid format. 10, +10, 10.0, 0.1E2, etc., all indicate a setting of plus 10 volts. When using binary, each voltage to be programmed is represented by a two byte value.

When purchased with the MATE option (Option 1M), the VX4730 complies with both the VXIbus Specification and the MATE IAC Standard. The module contains a TMA function that converts the DAC into a CIIL-speaking instrument and allows DC output voltage levels to be set up using CIIL commands.

The VX4730 incorporates extensive self test capabilities, with both visual and software indications of pass/fail status. The built-in self test determines that all twelve DAC channels are operational and that the programmed output voltages are accurate to within 3% of full scale.

During self test, each output is relay-isolated from the front panel connector to prevent possible damage to the Unit Under Test (UUT). A relay readback feature allows the closure status of each isolation relay to be determined. A self test failure of any of the twelve channels will cause the error LED to be lit and a discrete fault interrupt to be generated, indicating that an error message has been queued up.

On-board LEDs display the address status of the VX4730, monitor the presence of proper power on the power buses, indicate on-board failures, show syntax and other programming errors, and indicate which DAC channels have been programmed and have had their isolation relays closed.

Note that certain terms used in this manual have very specific meanings in the context of a VXIbus System. A list of these terms is presented in the VXIbus Glossary (Appendix C).

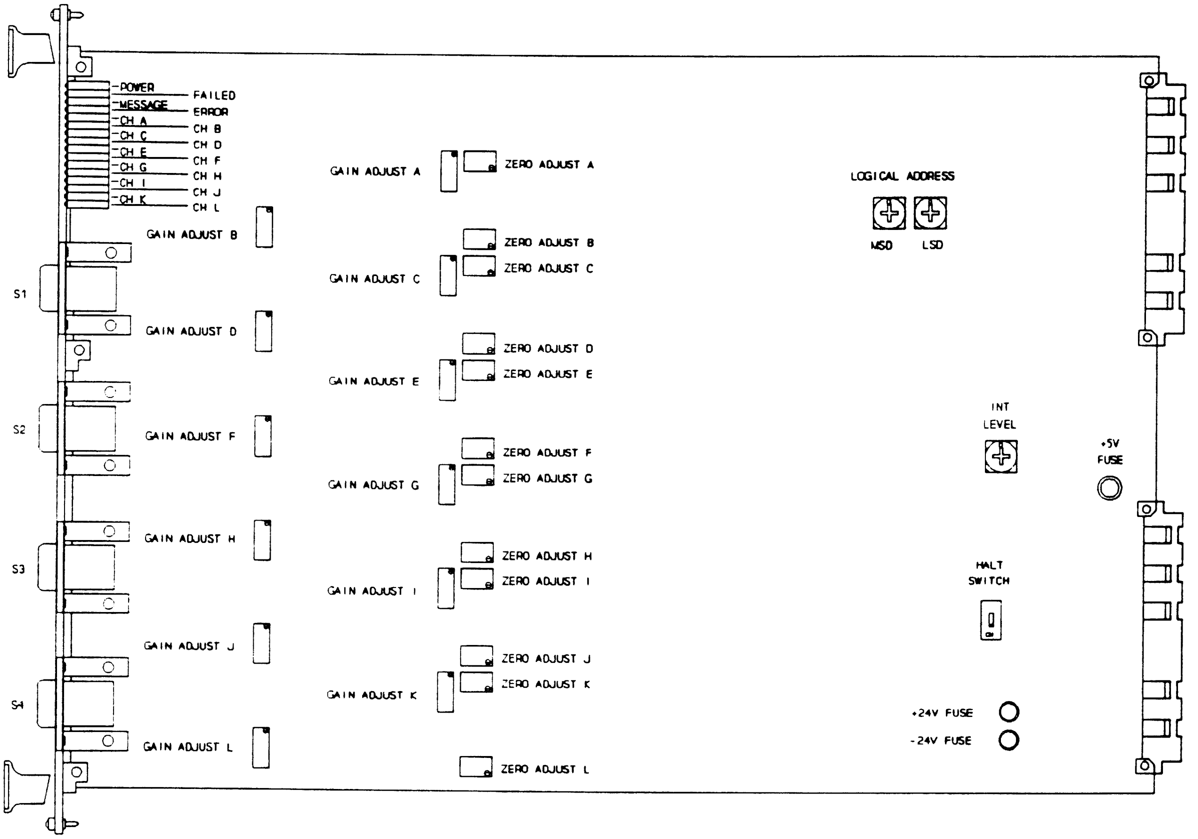


*Figure 1: VX4730 Controls and Indicators*

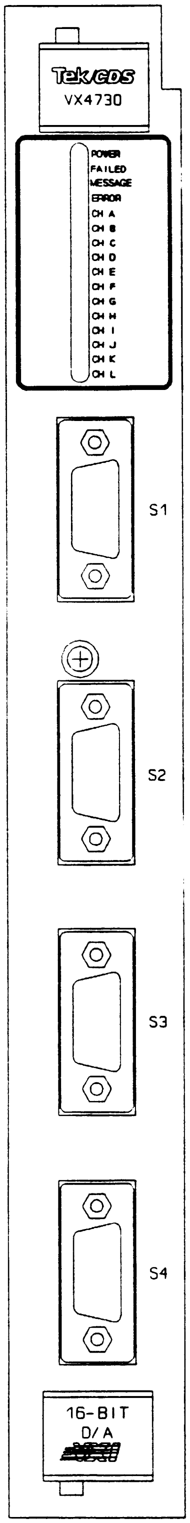


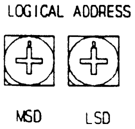
*Figure 2: VX4730 Front Panel*

## Controls And Indicators

The following controls and indicators are provided to select and display the functions of the VX4730 Module's operating environment. See Figures 1 and 2 for their physical locations.

### Switches

Logical Address Switches



Each function module in a VXIbus System must be assigned a unique logical address, from 1 to 255 decimal. The base VMEbus address of the VX4730 is set to a value between 1 and FFh (255d) by two hexadecimal rotary switches. Align the desired switch position with the arrow on the module shield.

The actual physical address of the VX4730 Module is on a 64 byte boundary. If the switch representing the most significant digit (MSD) of the logical address is set to position X and the switch representing the least significant digit (LSD) of the logical address is set to position Y, then the base physical address of the VX4730 will be [(64d * XYh) + 49152d]. For example:

|  | M | L |  |
|---|---|---|---|
| L. | S | S | Base Physical |
| A. | D | D | Addr. (d) |
| Ah | 0 | A | (64*10)+49152 = 49792d |
| 15h | 1 | 5 | (64*21)+49152 = 50496d |

where: L.A. = Logical Address
MSD = Most Significant Digit
LSD = Least Significant Digit

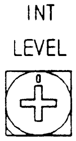
IEEE-488 Address

Using the VX4730 Module in an IEEE-488 environment requires knowing the module's IEEE-488 address in order to program it. Different manufacturers of IEEE-488 interface devices may have different algorithms for equating a logical address with an IEEE-488 address.

If the VX4730 is being used with a Tektronix/CDS IEEE-488 interface module, consult the operating manual of the Tektronix/CDS Resource Manager/IEEE-488 Interface Module being used.

If the VX4730 is being used in a MATE system, VXIbus logical addresses are converted to IEEE-488 addresses using the algorithm specified in the MATE IAC standard (MATE-STD-IAC). This algorithm is described in detail in the 73A-156 Operating Manual.

If the VX4730 is not being used with a Tektronix/CDS Resource Manager/IEEE-488 Interface Module, consult the operating manual of the IEEE-488 interface device being used for recommendations on setting the logical address.

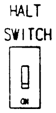


VMEbus Interrupt Level Select Switch

Each function module in a VXIbus System can generate an interrupt on the VMEbus to request service from the interrupt handler located on its commander. The VMEbus interrupt level on which the VX4730 Module generates interrupts is set by a BCD rotary switch. Align the desired switch position with the arrow on the module shield.

Valid Interrupt Level Select switch settings are 1 through 7, with setting 1 equivalent to level 1, etc. The level chosen should be the same as the level set on the VX4730's interrupt handler, typically the module's commander. Setting the switch to 0 or 8 will disable the module's interrupts. Switch setting 1 should not be used.

Interrupts are used by the module to return VXIbus Protocol Events to the module's commander. Refer to the Operation section for information on interrupts. The VXIbus Protocol Events supported by the module are listed in the Specifications section.



Halt Switch

This two-position slide switch selects the response of the VX4730 Module when the Reset bit in the module's VXIbus Control register is set. Control of the Reset bit depends on the capabilities of the VX4730's commander.

If the Halt switch is in the ON position, the VX4730 Module is reset to its power-up state and all programmed module parameters are reset to their default values.

If the Halt switch is in the OFF position, the module will ignore the Reset bit and no action will take place. Note that the module is not in strict compliance with the VXIbus Specification when the Halt switch is OFF.

## LEDs

The following LEDs are visible at the top of the VX4730 Module's front panel to indicate the status of the module's operation:

Power LED

This green LED is normally lit and is extinguished if the +5V power supply fails or if the +5V fuse blows.

Failed LED

This normally off red LED is lit whenever SYSFAIL* is asserted, indicating a module failure. Module failures include failure to correctly complete a self test, loss of a power rail, or failure of the module's central processor.

If the module loses any of its power voltages, the Failed LED will be lit and SYSFAIL* asserted. A module power failure is indicated when the module's Power LED is extinguished.

Message LED

This green LED is normally off. When lit, it indicates that the module is processing a VMEbus cycle. The LED is controlled by circuitry that appears to stretch the length of the VMEbus cycle. For example, a five microsecond cycle will light the LED for approximately 0.2 seconds. The LED will remain lit if the module is being constantly addressed.

Error LED
This red LED indicates that an error was found while attempting to execute a command sent to the VX4730. This includes out of range and syntax errors. The error that caused this LED to light can be determined by the ERR? (Error Query) command. The LED is cleared when the ERR? command is executed and all errors have been read.

Channel LEDs
These twelve green LEDs, labeled CH A through CH L, are lit if their respective channel has been programmed since the last reset or CLR command, and their associated isolation relay is closed. The isolation relay's true status is determined by a readback feature incorporated into this module, and is not simply based upon whether the relay was commanded to be open or closed.

Note that during self test all LEDs are turned on, even though their isolation relays remain open. Upon completion of self test, all LEDs revert back to their prior state.

### Fuses

The VX4730 Module has three fuses, for +5V, +24V and -24V. The fuses protect the module in case of an accidental shorting of the power bus or any other situation where excessive current might be drawn.

If the +5V fuse opens, the VXIbus Resource Manager will be unable to assert SYSFAIL INHIBIT on this module to disable SYSFAIL*.

If the +5V fuse opens, remove the fault before replacing the fuse. Replacement fuse information is given in the Specifications section.

### Isolation Relays

There is an isolation relay on each output. The relay allows the VX4730 to be completely isolated from the UUT under program control. Individual relays are controlled with the OPN and CLS commands. All isolation relays are in the open state when the system powers up (default). During self test these relays are automatically opened, then are returned to their previous state on completion of the self test.

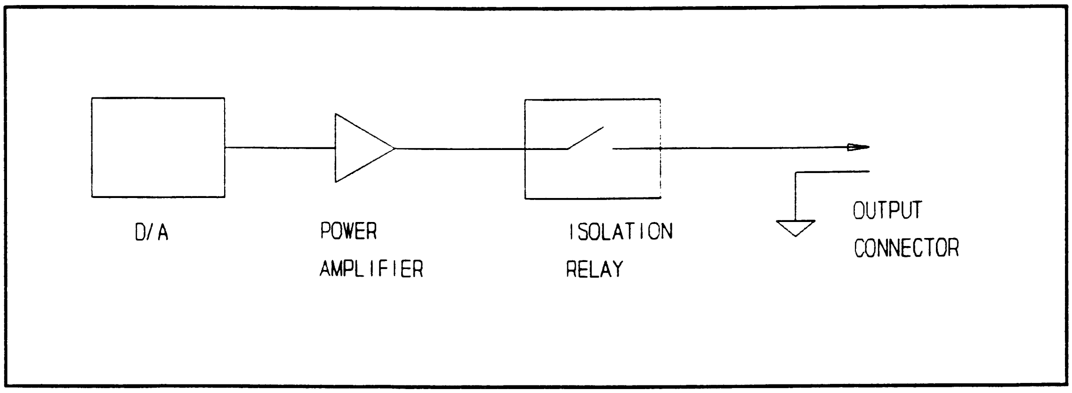


*Figure 3: Typical Output Channel*

## BITE (Built-In Test Equipment)

This module includes built-in self test capability that allows voltage outputs to be tested under internal program control. During self test, the voltage outputs of the module are isolated from the module's output connector by relays. Each output is compared with the output of another DAC, used as a reference, to assure it is within 3% of the programmed voltage. The comparison is performed over the entire voltage range from −16.3 to +16.3 volts. Two separate comparisons, each using a separate DAC as reference, are performed to increase the reliability of the test.

The module's built-in self test is initiated at power-up or when the IST (Internal Self Test) command is issued to the module.

In addition to the self test, this module incorporates a relay readback feature. The isolation relay position for each relay is indicated by an individual LED. Once a channel has been programmed, its channel LED indicates the true position of its isolation relay.

If a relay ever fails to go to its correct position when a CLS or OPN command is given, an error message will be queued up, the Error LED will turn on, and a Request True interrupt will be generated (if interrupts have been enabled with the INT command).

## Specifications

Function: 12 channel, 16-bit digital-to-analog convertor.

Digital-to-Analog Convertor Type: Single-ended, bipolar, 16-bit DAC.

Output:

Range: -16.3835 to +16.3835 volts.

Type: Single-ended.

Minimum Step Size: 0.5 millivolts.

Maximum Output Impedance: < 0.1 ohm, dc.

Short Circuit Duration: Continuous.

Current: 60 mA per channel, all channels driven. ±16.3835 V into a resistive load of 40 ohms or greater, single channel driven. All 12 outputs collectively must not exceed 720 mA.

Conversion Rate: Throughput is the maximum number of conversions per second which can be accomplished by the DAC on a continuous basis. The DAC is capable of in excess of 1000 voltage changes per second, all twelve channels, binary data, and 3000 voltage changes per second, single channel, binary data.

*NOTE*: The conversion time may also be limited by the system's interface module.

Settling Time: From the time the DAC value is programmed until the output has settled to within the specified percent of final value, 60 mA load.

Change of 32 V; 10 µs, 10%; 30 µs, 1%; 12 ms, 0.1%; 70 ms, 0.006%.

Change of 50 mV; 25 µs to within 1 mV of final value.

Accuracy: Guaranteed monotonic (0°C to 55°C), 14 bits.

Linearity Error: < ±1 mV @ 25°C.

Gain and Offset Error: Adjustable to ±0.5 mV with trim potentiometers.

Maximum Error With Time:

Percent of full scale at 25°C:

| | |
|---|---|
| 24 hrs. | ±0.009% |
| 30 days | ±0.014% |
| 90 days | ±0.023% |
| 6 mths | ±0.036% |
| 1 year | ±0.040% |

Temperature Coefficient: 0.3 mV per °C.

Self Test Accuracy: 3% or less of full scale range.

Modules per Mainframe: The number of modules allowed in a mainframe depends on the amount of current drawn from each channel and the current rating of the mainframe power supply. Refer to Appendix D to calculate the number of VX4730 Modules that may be installed in a mainframe.

VXIbus Compatibility: Fully compatible with the VXIbus Specification for message based instruments with the Halt switch in the ON position.

VXI Device Type: VXI message based instrument, VXIbus Revision 1.4

VXI Protocol: Word serial.

VXI Module Size: C size, one slot wide.

Module-Specific Commands: All module-specific commands and data are sent via the VXIbus Byte-Available command. All module-specific commands are made up of ASCII characters. Module-specific data may be in either ASCII or binary format.

VMEbus Interface: Data transfer bus (DTB) slave - A16, D16 only.

Interrupt Level: Switch selectable, levels 1 (highest priority) through 7 (lowest).

Interrupt Acknowledge: D16, lower 8 bits returned are the logical address of the module. Upper 8 bits contain the event or response code.

VXIbus Data Rate: Buffered mode write: 250K bytes/sec minimum binary or ASCII.
Nonbuffered mode write: 60K bytes/sec minimum binary data, 15 K bytes/sec ASCII Data.

VXIbus Commands Supported: All VXIbus commands are accepted (e.g. DTACK* will be returned). The following commands are recognized by this module; all other commands will cause an unrecognized command event.

ABORT NORMAL OPERATION
ASYNCHRONOUS MODE CONTROL
BEGIN NORMAL OPERATION
BYTE AVAILABLE (with or without END bit set)

BYTE REQUEST
CLEAR
CLEAR LOCK
CONTROL EVENT
CONTROL RESPONSE
END NORMAL OPERATION
GRANT DEVICE
IDENTIFY COMMANDER
READ INTERRUPTER LINE
READ INTERRUPTERS
READ PROTOCOL
READ PROTOCOL ERROR
SET LOCK
TRIGGER

VXIbus Protocol Events Supported:

VXIbus events are returned via VME interrupts. The following events are supported and returned to the VX4730 Module's commander:

> REQUEST TRUE (In IEEE-488 systems, this interrupt will cause a Service Request (SRQ) to be generated on the IEEE-488 bus.)

VXIbus Registers:

ID
Device Type
Status
Control
Protocol
Response
Data Low
See Appendix A for definition of register contents.

Power Requirements:

All required dc power is provided by the power supply in the VXIbus mainframe.

Voltage:

| | |
|---|---|
| +5 Volt Supply: | 4.75 V dc to 5.25 V dc. |
| +24 Volt Supply: | +23.2 V dc to +25.2 V dc. |
| -24 Volt Supply: | -23.2 V dc to -25.2 V dc. |

Current (Peak Module, $I_{PM}$):

| | |
|---|---|
| 5 volt supply: | 2.0 A |
| +24 volt supply: | 1.4 A |
| -24 volt supply: | 1.4 A |

Current (Dynamic Module, $I_{DM}$):

| | |
|---|---|
| 5 volt supply: | 0.243 A PTP |
| +24 volt supply: | 0.192 A PTP |
| -24 volt supply: | 0.304 A PTP |

Fuses:

Replacement fuse: Littlefuse P/N 273004; CDS P/N 42202-73040.

Cooling:

Provided by the fan in the VXIbus mainframe. Less than 5°C temperature rise (60 mA output current, all 12 channels) or less than

7°C rise with 1 channel at 150 mA output current with 3.5 liters/sec. of air at a pressure drop of 0.13 mm of $H_2O$.

Temperature:

0°C to +50°C, operating.
-40°C to +85°C, storage.

Humidity:

Less than 95% R.H. non-condensing, 0°C to +30°C.
Less than 75% R.H. non-condensing, +31°C to +40°C.
Less than 45% R.H. non-condensing, +41°C to +50°C.

Radiated Emissions:

Complies with VXIbus Specification.

Conducted Emissions:

Complies with VXIbus Specification.

Module Envelope Dimensions:

VXI C size. 262 mm x 353 mm x 30.5 mm (10.3 in x 13.9 in x 1.2 in).

Dimensions, Shipping:

When ordered with a Tektronix/CDS mainframe, this module will be installed and secured in one of the instrument module slots (slots 1 - 12).

When ordered alone, the card's shipping dimensions are:

406 mm x 305 mm x 102 mm.
(16 in x 12 in x 4 in).

Weight:

1.5 kg. (3.3 lbs.)

Weight, Shipping:

When ordered with a Tektronix/CDS mainframe, this module will be installed and secured in one of the instrument module slots (slots 1-12).

When ordered alone, the card's shipping weight is:

2 kg. (4.3 lb).

Mounting Position:

Any orientation.

Mounting Location:

Installs in an instrument module slot (slots 1-12) of a C or D size VXIbus mainframe. (Refer to D size mainframe manual for information on required adapters.)

Front Panel Signal Connectors:

Four DE-9S connectors, three channels on each connector. Refer to Appendix B for connector pinouts.

Recommended Cable:

VX1732P Analog cable (4 required for all 12 channels).

Equipment Supplied:

1 - VX4730 12-Channel D/A Module.

| | |
|---|---|
| Equipment Supplied: | 1 - VX4730 12-Channel D/A Module.<br>1 - Operating Manual (Part # 00000-34730).<br>1 - Service Manual (Part # 00000-44730). |
| Optional Equipment: | 4 - VX1732P Cables, or VX1784P Hooded Connectors. |
| Options: | Option 10: Delete six (6) channels of DACs.<br>Option 1M: MATE compatible CIIL command set. Complies with MATE-STD-2806763. |
| Software Version: | V2.6. |

# Section 2
# Preparation For Use

## Installation Requirements And Cautions

The VX4730 Module is a C size VXIbus instrument module and therefore may be installed in any C or D size VXIbus mainframe slot other than slot 0. If the module is being installed in a D size mainframe, consult the operating manual for the mainframe to determine how to install the module in that particular mainframe. Setting the module's Logical Address switch defines the module's programming address. Refer to the Controls and Indicators subsection for information on selecting and setting the module's logical address. To avoid confusion, it is recommended that the slot number and the logical address be the same.

### Tools Required

The following tools are required for proper installation:

Slotted screwdriver set.

**CAUTION**

*Note that there are two printed ejector handles on the card. To avoid installing the card incorrectly, make sure the ejector marked "VX4730" is at the top.*

*In order to maintain proper mainframe cooling, unused mainframe slots must be covered with the blank front panels supplied with the mainframe.*

Based on the number of instrument modules ordered with the mainframe, blank front panels are supplied to cover all unused slots. Additional VXIbus C size single-slot and C size double-slot blank front panels can be ordered from your Tektronix supplier.

**CAUTION**

*Verify that the mainframe is able to provide adequate cooling and power with this module installed. Refer to the mainframe Operating Manual for instructions.*

If the VX4730 is used in a VX1X Series Mainframe, all VX4730 cooling requirements will be met.

**CAUTION**

*If the VX4730 Module is inserted in a slot with any empty slots to the left of the module, the VME daisy-chain jumpers must be installed on the backplane in order for the VX4730 Module to operate properly. Check the manual of the mainframe being used for jumpering instructions.*

If a Tektronix/CDS VX1400 or VX1401 mainframe is being used, the jumper points may be reached through the front of the mainframe. There are five (5) jumpers that must be installed for each empty slot. The five jumpers are the pins to the left of the empty slot.

## Installation Procedure

**CAUTION**

*The VX4730 Module is a piece of electronic equipment and therefore has some susceptibility to electrostatic damage (ESD). ESD precautions must be taken whenever the module is handled.*

1) Record the revision level, serial number (located on the label on the top shield of the VX4730), and switch settings on the Installation Checklist. Only qualified personnel should perform this installation.

2) Verify that the switches are switched to the correct values. The Halt switch should be in the ON position unless it is desired to not allow the resource manager to reset this module.

   Note that with either Halt switch position, a "hard" reset will occur at power-up and when SYSRST* is set true on the VXIbus backplane. If the module's commander is a Tektronix/CDS Resource Manager/IEEE-488 Interface Module, SYSRST* will be set true whenever the Reset switch on the front panel of that module is depressed. Also note that when the Halt switch is in the OFF position, the operation of this module is not VXIbus compatible.

3) Make sure power is off in the mainframe.

4) The module can now be inserted into one of the instrument slots of the mainframe.

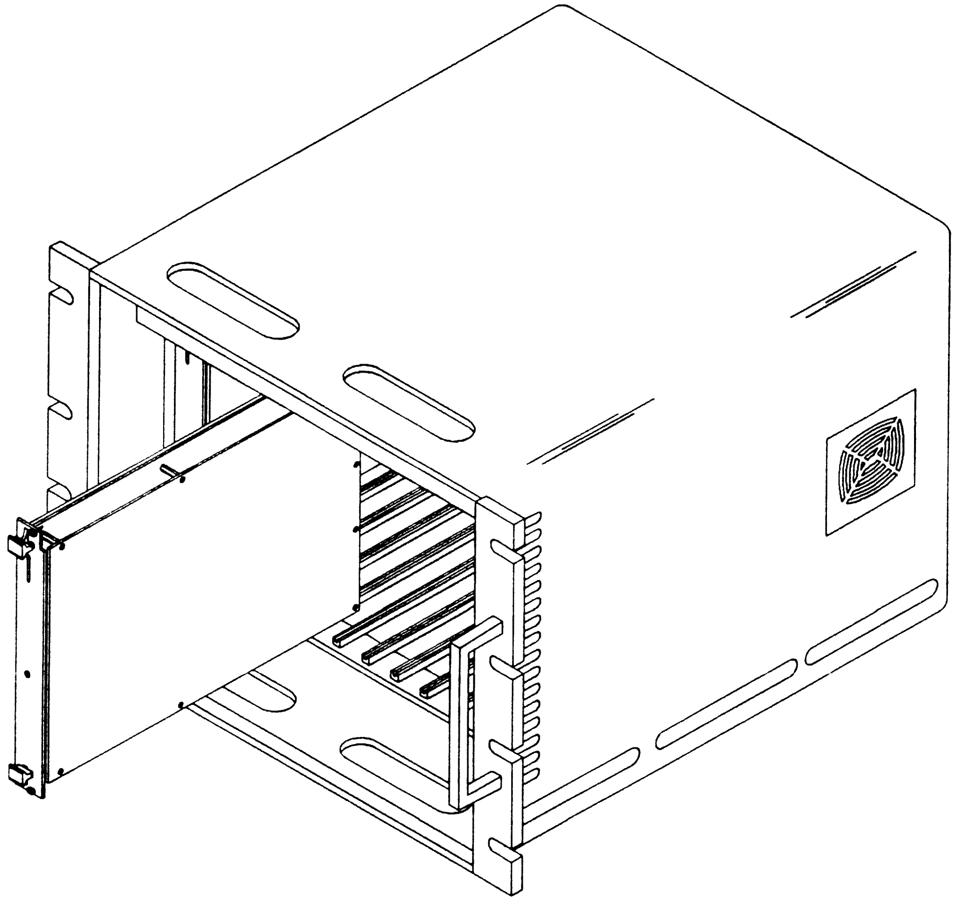


*Figure 4: Module Installation*

5) Cable Installation -

Use a VX1732 Cable to interface between the module I/O connector and the Unit Under Test (UUT). If the module is being installed in a Tektronix/CDS VX1400 or VX1401 Mainframe, route the cable from the front panel of the module down through the cable tray at the bottom of the mainframe and out the rear of the mainframe.

The mainframe is interfaced to the system controller using a standard IEEE-488 cable to connect the IEEE-488 connector on the rear panel of the VX1400 Mainframe to the IEEE-488 interface connector at the system controller.

## Installation Checklist

Installation parameters will vary depending on the mainframe being used. Be sure to consult the mainframe Operating Manual before installing and operating the module.

Revision Level: ____________________

Serial No.: ______________________

Mainframe Slot Number: _____________

Switch Settings:

VXIbus Logical Address Switch: ____________________

Interrupt Level Select Switch: ____________________

Halt Switch: ____________________

Cable / Hooded Connector Installed: ____________________

Performed by: ________________________ Date: _____________

# Section 3
# Operation

## Overview

The VX4730 consists of twelve (12) independent single-ended 16-bit DACs (digital-to-analog converters), individually programmable from -16.3835 volts to +16.3835 volts in 0.5 millivolt steps. Monotonicity is guaranteed to 14 bits.

Each output channel of the DAC provides a minimum of 60 milliamperes of current, with all channels driven. In addition, any individual channel may provide up to ±16.3835 V into a 40 Ohm load. The collective current for all twelve channels cannot exceed 720 milliamperes.

The VX4730 incorporates unique features which improve its speed and operational efficiency when installed in an ATE system. The Buffered mode automatically enables Fast Handshake protocol, a special provision of the VXIbus Specification that allows commands and/or data to be sent from the system controller to a module with minimum VXIbus protocol overhead. In this mode, the DAC stores incoming data/commands in an internal buffer that is sequentially processed. Module data processing and buffer loading occur simultaneously.

In non-buffered normal transfer mode, information is processed by the DAC on a byte-by-byte basis as it is received. This feature supports applications where it is important that the VX4730's operation remain synchronous with another event in the ATE system.

A combination of the benefits of both non-buffered mode and Fast Handshake mode can be obtained by sending binary data while in the non-buffered mode. In this case, information is processed a byte at a time, but the DAC automatically switches into Fast Handshake mode during the binary transfer.

The DAC may be programmed either in binary or by using ASCII character strings. When using ASCII, the channels to be programmed are specified first, and then the desired voltage level for each channel is specified in engineering units. (For example, "VAC 10,-2" sets channels A and C to 10.000 and -2.000 volts respectively). The voltage level may be indicated in any valid format. 10, +10, 10.0, 0.1E2, etc., all indicate a setting of plus 10 volts. When using binary, each voltage to be programmed is represented by a two byte value.

When purchased with the MATE option (Option 1M), the VX4730 complies with both the VXIbus Specification and the MATE IAC Standard. The module contains a TMA function that converts the DAC into a CIIL-speaking instrument and allows DC output voltage levels to be set up using CIIL commands.

The VX4730 Module is programmed by ASCII characters issued from the system controller to the VX4730 Module via the module's VXIbus commander and the VXIbus mainframe backplane. The module is a VXIbus Message Based Device and communicates using the VXIbus Word Serial Protocol. Refer to the manual for the VXIbus device that will be the VX4730 Module's commander for details on the operation of that device.

If the module's commander is a Tektronix/CDS Resource Manager/IEEE-488 Interface Module, refer to that Operating Manual and the programming examples in the Operation section of this manual for information on how the system controller communicates with the commander being used.

## Power-up

The VX4730 Module will complete its self test and be ready for programming three seconds after power-up. The Power LED will be on, and all other LEDs off. The MSG LED will blink briefly during the power-up sequence as the VXIbus Resource Manager addresses all modules in the mainframe. The default condition of the module after power-up is described in the SYSFAIL, Self test and Initialization subsection.

## System Commands

These low-level commands are typically sent by the module's commander, transparent to the user of the module. An exception is the Read STB command, which is sent whenever a Serial Poll on an IEEE-488 system is performed. Most commanders or Slot 0 devices have specific ASCII commands which will cause them to send one of these low-level commands to a specified instrument. Refer to the Operating Manual of the commander or Slot 0 device for information on these commands.

| Command | Effect |
|---|---|
| Clear | The module clears its VXIbus interface and any pending commands. Current module operations are unaffected. |
| Begin Normal Operation | The module will begin operation per VXI Specification. |
| Read Protocol | The module will return its protocol to its commander. |
| Read STB | The module will return its VXI status byte to its commander. |
| Set Lock | Set the Lock bit of the Response register. |
| Clear Lock | Clears the Lock bit of the Response register. |
| Read Interrupters | Returns the value FFF9, indicating there is one interrupter on this module. |

Read Interrupt Line
Returns the interrupt line per VXI Specification.

Asynchronous Mode Control
Returns information that events are being sent as interrupts per VXI Specification.

Abort Normal Operation
Causes this device to cease normal operation per VXI Specification.

End Normal Operation
Causes this device to cease normal operation per VXI Specification.

Control Event
Used by a commander to selectively enable the generation of events by a servant.

Read Protocol Error
Returns the module's most recent error code, which includes multiple query errors, unsupported commands, and DOR violations.

Byte Available
Transfers module commands to this module.

Byte Request
Requests data be returned form the module.

Control Response
Returns information indicating response interrupts are not supported.

Trigger
This module will accept the Trigger command, although no part of this instrument will be affected by it.

Grant Device
This module accepts this command, although it has no meaning to it because it has no servants.

Identify Commander
Sends the commander's logical address to this module.

## Module Commands

A summary of the VX4730 Module's commands is listed below. The summary also shows any required order of programming needed for commands. This is followed by detailed descriptions of each of the commands. A sample BASIC program using these commands is shown in the Programming Examples section.

*NOTE:*

*If Option 1M (MATE TMA) has been ordered with this module, see Appendix M for information on ATLAS/CIIL programming syntax. The commands listed in this section are not effective with the MATE option installed.*

### Command Syntax

Command protocol and syntax for the VX4730 Module are as follows:

1) Each command consists of a single line of any number of characters. Parameters may not be "wrapped around" (continued on the next line). Every command must end with a line-feed <LF> or semi-colon (;) terminator. The terminator may be omitted from any command if the End bit (which corresponds to the EOI signal in IEEE-488 systems) is set on the last character of the command. Carriage-returns <CR> are optional before line feeds or semicolons.

2) If a character is not enclosed by brackets, that character itself is sent, otherwise:

| | |
|---|---|
| [ ] | encloses the symbol for the actual argument to be sent. These argument symbols are defined under each command heading. |
| < > | indicates a binary value; ie: <0Ah> is a line feed. |
| <CR> | indicates a carriage-return. |
| <LF> | indicates a line-feed. |
| <SP> | indicates a space character. |
| <TM> | terminator: indicates a line-feed or a semicolon. |

3) Any character may be sent in either upper or lower case form.

4) Any of the following white space characters:

   00 hex
   01 hex through 08 hex
   09 hex (TAB character)
   0B hex through 19 hex (including carriage return)
   20 hex (SPACE character)

   are allowed in any of the following places:

   - before any comma, semicolon, or <LF>.
   - after any comma.
   - in place of any SPACE character listed on the syntax line in the command descriptions.

   Any number of white space characters may be used together.

5) Binary arguments must be formulated as follows:
   #0[$B_1$][$B_2$]...

   The '#0' characters are only required at the beginning od the binary string.

### Response Syntax

All responses end with a <CR><LF>, except where specified. The End bit is asserted with the <LF>. In the examples given in the command descriptions, the responses from the VX4730 are shown underlined.

| Command | Action |
|---|---|
| INT | Enables Request True interrupt generation. |
| BUF | Puts the module in buffered mode. |
| CLS | Closes the module's output isolation relay(s), connecting the output(s) of one or more DACs to the module's output connectors. |
| V | Programs the output voltage level of the specified DAC channel(s). Each DAC's output voltage changes as that channel's input is parsed. (See also the S command). |
| S | Programs the output voltage level(s) of the specified DAC channel(s). All outputs change simultaneously when the command terminator (semicolon or line feed) is parsed. (See also the V command). |
| A | Programs a single output voltage level for all DAC channels simultaneously. |
| D | Programs the output voltage level of the DAC channels specified in previous V, S, or A commands with ASCII characters. |
| B | Programs the output voltage level of the DAC channels specified in previous V, S, or A commands with binary data. |
| CLR | Clears all channel LEDs. **DEFAULT CONDITION.** |
| OPN | Opens the module's output isolation relay(s), disconnecting the output(s) of one or more DACs from the module's output connectors. **DEFAULT CONDITION.** |
| IST | Initiates the module's internal self test. |
| ERR? | Queries the error status of the module. |
| NBUF | Puts the module in nonbuffered mode. **DEFAULT CONDITION.** |
| DINT | Disables Request True interrupt generation. **DEFAULT CONDITION.** |
| RST | Resets the VX4730 to its power-up state. |
| REV? | Returns the VX4730's firmware revision level. |

A detailed description of each command, in alphabetical order, is given on the following pages.

## Command Descriptions

Command: A (Set voltage of all channels)

Syntax:

```
A z<TM>  (ASCII data format)
or
A #0z<TM>  (binary data format)
```

Purpose: The A command programs all channels to the specified output voltage.

Description: This command should be used when all outputs are to be programmed to the same value. It is important to note there is a time skew of approximately 11.5 µsec between the time that each output changes (from channel A to channel L), to prevent excessive dynamic current draw of this module.

z represents a voltage value that the DAC is to be programmed to. The data syntax may be either ASCII or binary, as defined in the V command.

This command also affects any subsequent B or D commands. The B or D commands are used when channel data and voltage data are to be given in separate commands. If the A command is sent, subsequent B or D commands will cause all channels to be programmed with the value specified by the B or D command.

Example: ASCII data format:

Any of the following would program all channels to +10.000 volts:

```
A +10.0<TM>
A +0.00000001E009<TM>
A 1000.00E-02<TM>
A .01e+3<TM>
A 10<TM>
```

Binary data format:

```
A #0<4Eh><20h><TM>
```

will also program all channels to +10.000 volts. An optional format for binary data, for time critical applications (the #0 characters need not be sent for this example) is as follows:

```
A<TM>
B <4Eh><20h><TM>
```

This would program all channels to +10.000 volts. For a complete description of how to program the VX4730 in a binary format, refer to the V command description. The <TM> termination character is optional in binary format.

Errors: If the value given is less than or equal to -16.38375 or greater than or equal to +16.38375, the module's Error LED will be lit and a VXIbus Request True event will be generated (if interrupts have been enabled with the INT command). Refer to the INT command for a complete description of VX4730 interrupts and to the ERR? command for the syntax of the error message.

Command: B (Program Binary Data)

Syntax: B $v_1v_2...v_{12}$<TM>

Purpose: Programs DAC channels using binary data.

Description: The B command programs the DAC outputs in the order specified by the last S, V, or A command. If the A command was sent, all channels will be programmed with the single voltage specified in this command. If the S command was sent, all channels are programmed when the terminator <TM> is parsed. If the V command was sent, all channels will be programmed as the v value is parsed. In nonbuffered mode, parsing occurs immediately on receipt of the character. The VXIbus is held off until parsing is complete. In buffered mode, parsing of the nth voltage occurs when all previously received characters have been processed.

The B command is used in situations where it is desirable not to send the channel information in the same command as the voltages, typically in speed-critical applications.

Each value of v has the form: [B1][B2]

No commas are used to delimit binary data. [B1] and [B2] represent a twos complement value with the least significant bit equivalent to 0.5 millivolts. Two bytes per channel must be sent to the 73A-256 in the binary format.

Some values in twos complement form are:

7FFF hex binary = 16.3835 volts (max)
0004 hex binary = 0.002 volts
0000 hex binary = 0.000 volts
fffc hex binary = -0.002 volts
8001 hex binary = -16.3835 volts (min)

*NOTE:* In the binary data format, both bytes must ALWAYS be sent for each channel specified by the previous S or V command. A single pair of bytes is sent for the A command. In non-buffered mode, the module automatically switches to the VXIbus Fast Handshake mode while receiving binary data if seven or more channels are being programmed with a single command.

Examples: SB<TM>
B <4Eh><20h><TM>

would program channel B to +10.000 volts.

SBJCG<TM>
B <4Eh><20h><B8h><18h><8Ah><D0h><00h><00h><TM>

would program channel B to 10.000 volts, channel J to -9.204 volts, channel C to -15.000 volts, and channel G to 0.000 volts.

The hex values within the right and left brackets < > represent a single 8-bit character. In other words, the <4Eh> in the example does not represent the five characters, '<','4','E','h', and '>', but rather the single byte character corresponding to 4E hex. The <TM> termination character is optional.

*NOTE:* In BASIC programming languages, a nonprintable binary byte is typically generated with the CHR$(X) function, where X is the decimal value 0 to 255 which represents the 8-bit binary data value.

Errors: If the value given is less than -16.38375 or greater than or equal to +16.38375, the module's Error LED will be lit and a VXIbus Request True interrupt will be generated (if interrupts have been enabled with the INT command). Refer to the INT command for a complete description of VX4730 interrupts and to the ERR? command for the syntax of the error message.

Command: BUF (Buffered input)

Syntax: BUF<TM>

Purpose: The BUF command allows the system controller to send data and commands to the VX4730 over the VXIbus at optimum speed, independent of the parsing and execution speed of this module.

Description: In the buffered mode, all data sent to the module is buffered before being parsed, allowing much faster transfer rates. This module operates using the VXIbus Fast Handshake mode while in buffered mode. See the Synchronizing Multiple Instrumentation Modules section for details on synchronizing multiple modules used in the buffered mode. The module can take in up to 4000 characters at the 400 Kbyte rate before it has to temporarily hold off the VXIbus.

*NOTE*: The following discussion applies only to users planning on sending extremely large amounts of data in a very short period of time (roughly more than 1000 voltage changes per second).

If you plan on sending 4000 bytes of data in under 200 milliseconds (which roughly corresponds to 50 µs/character, or 1000 changes in voltage per second) in buffered mode, the data will be received faster than the module's parser is able to process the characters, and eventually the module's 4096 byte buffer will fill up. This will cause a temporary VXIbus hold off condition, which is transparent except for the effect it has on data transfer speed. If the IEEE-488 controller is slower than the module's parser rate, as many are, this hold off condition would never be encountered.

When the hold off situation occurs, the VX4730 will not allow the VXIbus system controller to send any additional data until the parser has emptied half of its input buffer.

As an example, the first time the 4096 byte buffer is filled, the system controller will be held off until the first 2048 bytes are parsed. From this point on, every time the module releases the hold off condition, the controller may send another 2048 bytes, at which time it has to wait on the parser again.

Each character sent takes up one byte in the module input buffer unless the END bit is set (EOI for IEEE-488), in which case it takes up three bytes. All buffered VXIbus commands (Trigger, Set Lock, Clear Lock) take up three bytes. (The VXIbus commands Clear and Read Status are not buffered.) Refer to the VX4730's commander manual for information on generation of VXIbus commands.

Example: BUF<TM>

Command: CLR (Clear LEDs)

Syntax: CLR<TM>

Purpose: The Clear command clears (turns off) all channel LEDs.

Description: The CLR command turns off the twelve channel LEDs. The channel LEDs indicate which channels have been programmed since the last power-up or CLR command and also which channels have their isolation relays in the closed position. Once cleared, a channel LED will not turn on again until its channel is reprogrammed and its isolation relay is in the closed position.

*NOTE*: The CLR command has no effect on the actual output voltage of a channel or the status (open/closed) of a channel's isolation relay.

Example: CLR<TM>

Command: CLS (Close Isolation Relays)

Syntax: CLS $z_1,\ldots,z_n$<TM>

Purpose: The Close command connects the specified channel(s)' DAC output to the module's output connector.

Description: The $z_1$ represents the channel(s), A through L, whose isolation relays are to be closed. If no channel is specified, all channels' outputs are connected to the module's output connector.

Examples: CLS A,B<TM>

CLS <TM>

The first example closes the isolation relay for both channels A and B, while the second example closes all channel isolation relays.

Errors: If the command contains syntax errors, such as CLS N<TM> (close the isolation relay of an undefined channel), then the module's Error LED will be lit and a VXIbus Request True event will be generated (if interrupts have been enabled with the INT command). Refer to the INT command for a complete description of VX4730 interrupts and to the ERR? command for the syntax of the error message.

Command: D (Program ASCII Data)

Syntax: D $v_1, v_2, \ldots v_{12}$<TM>

Purpose: Programs DAC channels using ASCII data.

Description: The D command programs the DAC outputs in the order specified by the last S, V, A command. If the A command was sent, all channels will be programmed with the single voltage specified in this command. If the S command was sent, all channels are programmed when the terminator <TM> is parsed. If the V command was sent, all channels will be programmed as the v value is parsed. In nonbuffered mode, parsing occurs immediately on receipt of the character. The VXIbus is held off until parsing is complete. In buffered mode, parsing of the nth voltage occurs when all previously received characters have been processed.

The D command is used in situations where it is desirable not to send the channel information in the same command as the voltages, typically in speed-critical applications.

v represents the voltage that a DAC channel(s) are to be programmed to.

There must be one v for every channel specified in the last S, V, or A command (specify one v for the A command). The format for each v may be integer, decimal, or scientific notation. The format of a scientific notation number is as follows:

$$\pm E_1E_2.E_3E_4E_5E \pm E_6E_7E_8$$

The integer and fractional portion of the mantissa may be of any length, but the exponent portion, if included, is limited to three digits.

ASCII data values must be delimited by commas. Examples of ASCII data formats are shown in the Examples below.

Examples: Any of the following would program channel B to +10.000 volts:

```
SB<TM>
D +10.0<TM>
D +0.00000001E009<TM>
D 1000.00E-02<TM>
D .01e+3<TM>
D 10<TM>
```

Errors: If the value given is less than -16.38375 or greater than or equal to +16.38375, the module's Error LED will be lit and a VXIbus Request True interrupt will be generated (if interrupts have been enabled with the INT command). Refer to the INT command for a complete description of VX4730 interrupts and to the ERR? command for the syntax of the error message.

Command: DINT (Disable Interrupts)

Syntax: DINT<TM>

Purpose: This command disables generation of the VXIbus Request True event when an error condition is detected by this module.

Description: The DINT command stops the VX4730 from generating any external interrupts on the VXIbus that could be caused by a module error condition. If interrupts are not disabled and the VX4730 detects a programming error or self test error, it has the capability to generate a VXIbus Request True event to its interrupt handler (typically its commander).

For further information on VX4730 programming errors, refer to the ERR? command.

Example: DINT<TM>

Command: ERR? (Report errors)

Syntax: ERR?<TM>

Purpose: The ERR? command instructs this module to return its error status the next time input is requested from the module.

Description: This command is typically issued to the module in response to a VXIbus Request True event (in an IEEE-488 system, the Request True event generates an SRQ on the IEEE-488 bus). Errors reported by this command include those detected during self test and programming errors.

All errors listed in this section cause a Request True interrupt to be generated if interrupts are enabled via the INT command.

All errors occurring since the last ERR? command or reset condition will be returned, beginning with the first error that occurred. After issuing the ERR? command to the module, the system controller should continue to request input from the module until the "0,0,NO ADDITIONAL ERRORS TO REPORT" message is returned from the module.

The ERR? command is compatible with the standard "send query command/read response data" method as defined in the 488.2 specification for querying an instrument. Sending the ERR? command before reading the response is entirely optional. Whenever a response is read, error data will be returned.

Response Syntax: The format of data returned by the ERR? command is:

```
[channel ID],[error],[ASCII message]<CR><LF>
[channel ID],[error],[ASCII message]<CR><LF>
.
.
.
0,0, NO ADDITIONAL ERRORS TO REPORT <CR><LF>
```

where:

[channel ID] is one of the following ASCII characters:

| | |
|---|---|
| A - L | - error occurred on this channel |
| Z | - error is a channel independent error |
| 0 | - no additional errors to report |

[error] is a 1 digit error code.

[ASCII message] is an English message describing the error.

The meaning of [error] depends upon the [channel ID]. If the error message [channel ID] is a 0, either all errors have been reported or no errors have occurred since the last ERR? command or reset.

All possible values for [error] and [ASCII message] are listed below. [error] is listed first, with [ASCII message] below it, and below this the description of the error.

[channel ID] = 0

Error # = 0
NO ADDITIONAL ERRORS TO REPORT

There are no more errors to report. [error] is always 0 for [channel ID] = 0.

[channel ID] = A through L

Error # = 1
SELF TEST FAILURE: VOLTAGE OUTPUT DOES NOT CHANGE

Although different voltage values were programmed, the channel's DAC did not change value during self test.

Error # = 2
SELF TEST FAILURE: BAD OUTPUT VOLTAGE

The output voltage changed during self test but was not within 3% or 1/2 volt of the required value.

Error # = 3
VOLTAGE OVERRANGE

The data value sent in conjunction with the V, S, or A command was too large. This error occurs if the value sent is greater than or equal to +16.38375 volts.

Error # = 4
VOLTAGE UNDERRANGE

The data value sent in conjunction with the V, S, or A command was too small. This error occurs if the value sent is less than -16.38375 volts.

Error # = 5
[CMD] COMMAND WITH VOLTAGE OMITTED

This error occurs when a channel is specified without a corresponding voltage. [CMD] = V, S, or A command, indicating the command that generated the error.

Error # = 6
TOO MANY DIGITS IN EXPONENT

This error occurs if the exponent of the voltage value exceeds three digits.

Error # = 7
RELAY STAYS IN CLOSED POSITION

This error occurs when an isolation relay stays in the closed position after receiving an OPN command.

Error # = 8
RELAY STAYS IN OPEN POSITION

This error occurs when an isolation relay stays in the open position after receiving a CLS command.

Error # = 9
[CMD] COMMAND WITH CHANNEL OMITTED

This error occurs when a V or S command is received without indicating the channel to be programmed. [CMD] = V or S command, indicating the command that generated the error.

<u>[channel ID] = Z</u>

Error # = 1
RECEIVED UNEXPECTED [CHR] WHILE [REASON]

Where:

[CHR] = [single quote][character][single quote] for printable characters (20 hex through 7F hex), for example, 'G'.
or
[CHR] = [sp][ASCII hex digit][ASCII hex digit] for nonprintable characters (00 hex through 19 hex and 80 hex through FF hex), for example, 0A .

[REASON] = one of the following:
- EXPECTING A LINE FEED, SEMICOLON OR COMMA.
- EXPECTING A VOLTAGE.
- PARSING MANTISSA.
- PARSING EXPONENT.
- EXPECTING A CHANNEL CHARACTER.

Error # = 2
UNRECOGNIZED COMMAND

This error occurs if a command that is not listed in this document is received by the module.

Error # = 3
TOO MANY CHANNELS SPECIFIED (MAX OF 12)

This error occurs when more than twelve channels have been specified.

Examples: ERR?<TM>

Example Responses:

no errors:

```
0,0,NO ADDITIONAL ERRORS TO REPORT<CR><LF>
```

multiple errors:

```
A,2,SELF TEST FAIL...<CR><LF>
B,1,SELF TEST FAIL...<CR><LF>
A,3,VOLTAGE OVERRANGE<CR><LF>
Z,1,RECEIVED UNEXPECTED 'C' WHILE PARSING
EXPONENT<CR><LF>
0,0,NO ADDITIONAL ERRORS TO REPORT<CR><LF>
```

Command: INT (Interrupt enable)

Syntax: INT<TM>

Purpose: The INT command enables generation of the VXIbus Request True event when an error condition is detected by this module.

Description: The INT command enables the module to generate a VXIbus Request True event whenever any of the error conditions listed under the ERR? command occur. If the module is installed in an IEEE-488 system, the occurrence of a VXIbus Request True event condition will cause a Service Request (SRQ) to be generated on the IEEE-488 bus.

Example: INT<TM>

Command: IST (Internal Self Test)

Syntax: IST<TM>

Purpose: The IST command initiates an internal self test of this module.

Description: This command performs an instrument self test.

All outputs are first isolated from the module's front panel connector.

Each of eleven of the DAC's outputs are compared to the twelfth, which is used as a reference, during this self test. The test is then repeated, using a different DAC as reference.

If the self test detects a channel more than 3% out of tolerance, the ERR LED will be lit, and a message describing the failure will be queued up to be returned to the module's commander in response to the ERR? command. The module is still operational in this state.

If the module passes the self test, the message '0,NO ADDITIONAL ERRORS TO REPORT' will be returned in response to the ERR? command.

At the completion of self test, the module is returned to its pre-test state.

Example: IST<TM>

Command: NBUF (Nonbuffered Mode)

Syntax: NBUF<TM>

Purpose: The NBUF command puts the module into the nonbuffered mode of operation.

Description: In the nonbuffered mode, a byte of command/data is not accepted from the VXIbus until the previous character has been processed. By using this mode, the VX4730 maintains synchronization with its commander, and the user knows that the DAC has been programmed when the acceptance of the second byte after the last digit of the voltage level occurs. For example, if <CR><LF> is used as a terminator, it is guaranteed that the programmed voltage is at the output connector when the <LF> is accepted.

The major advantage of this method is that another module which may use the output of the VX4730 can immediately be programmed after the VX4730. Consult Synchronizing Multiple Instrumentation Modules at the end of this section for more details.

*NOTE*: The following paragraph only applies to the programmer who will be switching back and forth between buffered and nonbuffered mode.

It is important to note that since this command typically will be received while the module is in the Buffered mode, it will not take effect until the processor has parsed it (receiving characters and processing them occur independently in buffered mode). To guarantee that the module is actually in Nonbuffered mode before executing another command, a query command (i.e. ERR? or REV?) should be sent to the VX4730 after the NBUF command and the result read. This will re-synchronize the module and the controller, since the response to the query is not returned until both the NBUF and ERR? or REV? commands have been processed.

Example: NBUF<TM>

Command: OPN (Open Isolation Relays)

Syntax: OPN $z_1,\ldots,z_n$<TM>

Purpose: The OPN command physically disconnects the specified channel(s)' DAC from the module's output connector using a relay.

Description: z represents the channel(s), A through L, whose isolation relays are to be opened.

If no channels are specified, all channels are disconnected from the module's output connector. This command does not affect any programmed voltages.

Examples: OPN A,B<TM>

OPN <TM>

The first example opens the isolation relay for both channels A and B, while the second example opens all isolation relays.

Errors: If the command contains syntax errors, such as OPN W<TM> (open the isolation relay of an undefined channel), then the module's Error LED will be lit and a VXIbus Request True interrupt will be generated (if interrupts have been enabled with the INT command). Refer to the INT command for a complete description of VX4730 interrupts and to the ERR? command for the syntax of the error message.

Command: REV? (Revision Level)

Syntax: REV?<TM>

Purpose: The REV? command instructs the module to return the revision level of the onboard microprocessor firmware.

Description: This command returns the revision level of the onboard firmware as an alphanumeric string representing the revision level.

Example: REV?<TM>

Response Syntax: An example of a typical response is:

REVISION 1.0<CR><LF>

Command: RST (Reset)

Syntax: RST<TM>

Purpose: The Reset command resets the module to its power-up state.

Description: When the RST command is received, the module is reset to its power-up state:

| | |
|---|---|
| Isolation: | Open |
| D/A Output: | 0.000V |
| Input Mode: | Non-buffered |
| Interrupts: | Disabled |

Command: S (Simultaneously Set Voltage)

Syntax: $Sz_1z_2...z_{12}$ $v_1,v_2,...,v_{12}$<TM> (ASCII data format)
or
$Sz_1z_2...z_{12}$ #0$v_1v_2...v_{12}$<TM> (binary data format)
or
$Sz_1z_2...z_{12}$<TM> (channel setup only)

Purpose: The S command sets up the order in which channels are programmed, and then, when the voltages are specified (in this command or in subsequent B or D commands), programs all specified DAC channels to their specified voltages simultaneously.

Description: When the voltages are given (either in this command or in a subsequent B or D command), the outputs of the DACs change together with the parsing of the command terminator <TM> of the command specifying the voltages. Although this command is used when the specified outputs are to change together, it is important to note there is a time skew of approximately 11.5 µsec between the time that each output changes (in the same order the channels are given), to prevent excessive dynamic current draw of this module.

z represents the DAC channel (A through L) to be programmed.

v if given, represents the voltage that a DAC channel is to be programmed to, given in the same order as the channel characters.

From 1 to a maximum of 12 channels may be specified in a single command. Note that there is no space between the S and the [z] characters, and a space is required before the specified voltages.

If no voltages are specified, the command acts only to specify the channel ordering for a subsequent D or B command, and to specify that channels are to be updated together on reception of the <TM> terminator of the D or B command.

If voltages are specified, there must be one v for every z, with the first v separated from the last z by a white space character. This value may be in one of two formats, the ASCII format or the binary format.

The ASCII data format for each v may be integer, decimal, or scientific notation. The format of a scientific notation number is as follows:

$$\pm E_1E_2.E_3E_4E_5E \pm E_6E_7E_8$$

The integer and fractional portion of the mantissa may be of any length, but the exponent portion, if included, is limited to three digits.

ASCII data values must be delimited by commas. Examples of ASCII data formats are shown in the Examples below.

The binary data format for each v is: #0$B_1B_2$

The characters "#0" are only required at the beginning of the binary string. No commas are used to delimit binary data. [B1] and [B2] represent a twos complement value with the least significant bit equivalent to 0.5 millivolts. Two bytes per channel must be sent to the VX4370 in the binary format.

Some values in twos complement form are:

7FFF hex binary = 16.3835 volts (max)
0004 hex binary = 0.002 volts
0000 hex binary = 0.000 volts
fffc hex binary = -0.002 volts
8001 hex binary = -16.3835 volts (min)

*NOTE:* In the binary data format, both bytes must ALWAYS be sent for each value. In non-buffered mode, the module automatically switches to the VXIbus Fast Handshake mode while receiving binary data if seven or more channels are being programmed with a single command.

Examples: ASCII data format:
Any of the following would program channel B to +10.000 volts:

```
SB +10.0<TM>
SB +0.00000001E009<TM>
SB 1000.00E-02<TM>
SB .01e+3<TM>
SB 10<TM>

SB<TM>
D +10.0<TM>
```

```
SBJCG +10.0 ,-9.204, -0.15e+2,0<TM>
```

will program channel B to 10.000 volts, channel J to -9.204 volts, channel C to - 15.000 volts, and channel G to 0.000 volts.

Binary data format:

```
SB #0<4Eh><20h><TM> and
SBJCG #0<4Eh><20h><B8h><18h><8Ah><D0h><00h><00h><TM>
```

would have the same results as the ASCII data format examples above. An optional method of programming binary data is as follows:

```
SB<TM>
B <4Eh><20h><TM>
SBJCG<TM>
B <4Eh><20h><B8h><18h><8Ah><D0h><00h><00h><TM>
```

The hex values within the right and left brackets < > represent a single 8-bit character. In other words, the <4Eh> in the example does not represent the five characters, '<','4','E','h', and '>', but rather the single byte character corresponding to 4E hex. The <TM> termination character is optional in binary format.

*NOTE:* In BASIC programming languages, a nonprintable binary byte is typically generated with the CHR$(X) function, where X is the decimal value 0 to 255 which represents the 8 bit binary data value.

Errors: If the value given is less than -16.38375 or greater than or equal to +16.38375, the module's Error LED will be lit and a VXIbus Request True interrupt will be generated (if interrupts have been enabled with the INT command). Refer to the INT command for a complete description of VX4370 interrupts and to the ERR? command for the syntax of the error message.

Command: V (Set Voltage)

Syntax: $Vz_1z_2...z_{12}$ $v_1,v_2,...v_{12}$<TM> (ASCII data format)
or
$Vz_1z_2...z_{12}$ $\#0v_1v_2...v_{12}$ (binary data format)
or
$Vz_1z_2...z_{12}$<TM> (channel setup only)

Purpose: The V (Set Voltage) command sets up the order in which channels are programmed, and then, when the voltages are specified (in this command or in subsequent B or D commands), programs all specified DAC channels to their specified voltages.

Description: When the voltages are given (either in this command or in a subsequent B or D command), the outputs of the DACs change as each v value is parsed. In nonbuffered mode, parsing occurs immediately upon receipt of the character. The VXIbus is held off until parsing is complete. In buffered mode, parsing of the nth voltage occurs when all previously received characters have been processed. Use the S command if the application requires all outputs to change together with the command terminator.

z represents the DAC channel (A through L) to be programmed.

v represents the voltage that a DAC channel is to be programmed to, given in the same order as the channel characters.

From 1 to a maximum of 12 channels may be programmed with a single command. Note that there is no space between the V and the [z] characters.

If no voltages are specified, the command acts only to specify the channel ordering for a subsequent D or B command, and to specify that channels are to be updated as the voltages are parsed in the D or B command.

If voltages are specified, there must be one v for every z, with the first v separated from the last z by a white space character. This value may be in one of two formats, the ASCII format or the binary format.

The ASCII data format for each v may be integer, decimal, or scientific notation.

The format of a scientific notation number is as follows:

$$\pm E_1E_2.E_3E_4E_5E \pm E_6E_7E_8$$

The integer and fractional portion of the mantissa may be of any length, but the exponent portion, if included, is limited to three digits.

ASCII data values must be delimited by commas. Examples of ASCII data formats are shown in the Examples below.

The binary data format for each v is: #0$B_1B_2$

The characters "#0" are only required at the beginning of the binary string. No commas are used to delimit binary data. [$B_1$] and [$B_2$] represent a twos complement value with the least significant bit equivalent to 0.5 millivolts. Two bytes per channel must be sent to the VX4730 in the binary format.

Some values in twos complement form are:

```
7FFF hex binary = 16.3835 volts (max)
0004 hex binary = 0.002 volts
0000 hex binary = 0.000 volts
FFFC hex binary = -0.002 volts
8001 hex binary = -16.3835 volts (min)
```

*NOTE*: In the binary data format, both bytes must ALWAYS be sent for each value. While in non-buffered mode, the module automatically switches to the VXIbus Fast Handshake mode while receiving binary data if seven or more channels are being programmed with a single command.

Examples: ASCII data format: any of the following will program channel B to +10.000 volts:

```
VB +10.0<TM>
VB +0.00000001E009<TM>
VB 1000.00E-02<TM>
VB .01e+3<TM>
VB 10<TM>

VB<TM>
D +10.0<TM>
```

```
VBJCG +10.0 ,-9.204, -0.15e+2,0<TM>
```

will program channel B to 10.000 volts, channel J to -9.204 volts, channel C to -15.000 volts, and channel G to 0.000 volts.

Binary data format:

```
VB #0<4Eh><20h><TM>
VBJCG
#0<4Eh><20h><B8h><18h><8Ah><D0h><00h><00h><TM>
```

will have the same results as the ASCII data format examples above. An optional method of programming binary data is as follows:

```
VB<TM>
B <4Eh><20h><TM>
VBJCG<TM>
B <4Eh><20h><B8h><18h><8Ah><D0h><00h><00h><TM>
```

The hex values within the right and left brackets < > represent a single 8-bit character. In other words, the <4Eh> in the example does not represent the five characters, '<', '4','E', 'h', and '>', but rather the character corresponding to 4E hex. The <TM> termination character is optional in binary format.

*NOTE*: In BASIC programming languages, a nonprintable binary byte is typically generated with the CHR$(X) function, where X is the decimal value 0 to 255 which represents the 8 bit binary data value.

Errors: If the value given is less than or equal to -16.38375 or greater than or equal to +16.38375, the module's Error LED will be lit and a VXIbus Request True interrupt will be generated (if interrupts have been enabled with the INT command). Refer to the INT command for a complete description of VX4730 interrupts and to the ERR? command for the syntax of the error message.

## SYSFAIL, Self Test, and Initialization

The VX4730 Module will execute a self test at power-up, or upon direction of a VXIbus hard or soft reset condition, or upon command. The power-up self test consists of an interface self test and an instrument self test. A VXIbus hard reset occurs when another device, such as the VXIbus Resource Manager, asserts the backplane line SYSRST*. A VXIbus soft reset occurs when another device, such as the VX4730's commander, sets the Reset bit in the VX4730's Control register.

At power-up, as well as during self test, all module outputs remain isolated from the module's front panel connector.

During a power-up, or hard or soft reset, the following actions take place:

1) The SYSFAIL* (VME system-failure) line is set active, indicating that the module is executing an interface self test, and the Failed LED is lit. In the case of a soft reset, SYSFAIL* is set. However, all Tektronix/CDS commanders, such as the VX4521, will simultaneously set SYSFAIL INHIBIT. This is done to prevent the resource manager from prematurely reporting the failure of a card.

2) On completion of the interface self test, SYSFAIL* is de-asserted. If the test fails, the SYSFAIL* line remains active. If the interface self test passed, the SYSFAIL* line is released, and the module enters the VXIbus PASSED state (ready for normal operation). If it failed, the module enters the VXIbus FAILED state.

3) The instrument self test, as described in the IST command, is then executed. This relay-isolated test tests all DAC outputs within 3% accuracy. If the self test fails, the module makes an internal record of what failures occurred. This record will be returned in response to the ERR? command.

The default condition of this module after the completion of a power-up or a hard or soft reset self test is as follows:

| | |
|---|---|
| Isolation: | Open |
| D/A Output: | 0.000V |
| Input Mode: | Non-buffered |
| Interrupts: | Disabled |

The self test can be run at any time during normal operation by using the IST command. At the end of a self test initiated by the IST command, the module is restored to its pre-test state.

For example, if Channel A is programmed to +16V with its isolation relay closed, after the commanded self test is complete the channel will be reprogrammed to +16V and its relay closed.

During a commanded self test (IST command):

1) SYSFAIL* is not asserted.

2) The module executes the same instrument self test as described for power-up self test.

3) When the self test is completed, the module restores itself to its pre-test state. If the test fails, the ERR LED will be lit and relevant error messages will be queued for reporting with the ERR? command.

### SYSFAIL* Operation

SYSFAIL* becomes active on a software failure, during power-up, a hard or soft reset, or if the module loses +5 or ±24 volt power. When the mainframe Resource Manager detects SYSFAIL* set, it will attempt to inhibit the line. This will cause the VX4730 Module to deactivate SYSFAIL* in all cases except when +5 volt power is lost.

## Synchronizing Multiple Instrumentation Modules

When designing a test procedure, it is important to take into account the problems that can arise if the individual instrument modules are not properly synchronized. For example, if a relay on one module switches a signal to a voltmeter on another module, and the voltmeter reads the value before the relay has settled, an improper reading will result.

There are two primary methods of implementing proper synchronization:

1) One is to send data to one or more modules as quickly as possible and then check to see if all on-module operations are complete before performing the secondary operation (for example, reading the voltage).

2) The second method is to have the module hold off the data coming from the controller until the on-module operation is complete. In this case, the voltmeter can be read immediately after the first module is programmed.

The particular application generally determines the method used. The first method results in faster throughput, but requires that some kind of polling sequence take place to assure that on-module operations are complete. The second method is easier to implement and insures that no module will be programmed before operations on a previously addressed module are complete. However, this method may cause one module to hold up data transfer during an interval when other modules could be programmed.

The VX4730 allows you to use either method. The first method can be initiated by sending the BUF (buffered mode) command, which allows data collection and data processing to occur in parallel, thus allowing optimal data transfer rates. The VXI Fast Handshake protocol is used during this time. To be sure that VX4730 operations are complete, send the ERR? or REV? command and then read the response. The response will not be returned until all commands in the VX4730's input buffer have been executed.

The second method uses the default setting on the VX4730, the nonbuffered mode. For V, S, A, B, or D commands, this means that the output will be programmed to the specified value upon the module's acceptance of the second byte after the last digit of a numeric value. If a <CR><LF> is used to terminate the command, this corresponds to the <LF>. If a semicolon is used for termination, either a space following the semicolon or two semicolons without a space between them can be sent.

The VX4730 settling time should be referenced to see how much delay is needed for the output to settle to the desired accuracy before any subsequent instrument measurement which is dependent on the voltage output takes place. For all commands other than V, S, A, B, or D commands, operations are guaranteed to be complete before the first character of the next command will be accepted.

When using synchronized nonbuffered mode, it is important that the slot 0 module maintain byte-to-byte synchronization between modules.

Increased throughput in non-buffered mode can be obtained by sending data in binary format to gain some of the advantages of both methods. In this mode, the data bypasses the onboard processor and is transferred directly to the DACs which are being programmed. Binary format is also accepted in buffered mode. However, some of its advantages are lost because the data is buffered before being sent to the DACs.

# Section 4
# Programming Examples

This section contains example programs which demonstrate how some of the various programmable features of the VX4730 are used. The examples are written in BASIC using an IBM PC or equivalent computer as the system controller, using National Instruments GPIB calls.

## Definition of BASIC Commands

The programming examples in this manual are written in Microsoft GW BASIC. These examples use the GW BASIC commands described below. If the programming language you are using does not conform exactly to these definitions, use the command in that language that will give the same result.

Command — Result

CALL IBRD — The CALL IBRD statement inputs data into the string R$ from the IEEE-488 instrument whose decimal primary address is contained in the variable ADDRESS%. Following the input, the variable LENGTH% contains the number of bytes read from the instrument. The variable STATUS% contains the number '0' if the transfer was successful or an '8' if an operating system timeout occurred in the PC. Prior to using the CALL IBRD statement, the string R$ must be set to a string of spaces whose length is greater than or equal to the maximum number of bytes expected from the VX4730.

CALL IBWRT — The CALL IBWRT statement outputs the contents of the string variable WRT$ to the IEEE-488 instrument whose decimal primary address is contained in the variable ADDRESS%. Following the output of data, the variable STATUS% contains a '0' if the transfer was successful and an '8' if an operating timeout occurred in the PC.

END — Terminates the program.

FOR/NEXT — Repeats the instructions between the FOR and NEXT statements for a defined number of iterations.

GOSUB n — Runs the subroutine beginning with line n. EX: GOSUB 750 - runs the subroutine beginning on line 750. The end of the subroutine is delineated with a RETURN statement. When the subroutine reaches the RETURN statement, execution will resume on the line following the GOSUB command.

GOTO n

Program branches to line n. EX: GOTO 320 - directs execution to continue at line 320.

IF/THEN

Sets up a conditional IF/THEN statement. Used with other commands, such as PRINT or GOTO, so that IF the stated condition is met, THEN the command following is effective. EX: IF I = 3 THEN GOTO 450 - will continue operation at line 450 when the value of variable I is 3.

REM or '

All characters following the REM command are not executed. REM statements are used for documentation and user instructions. EX: REM **CLOSE ISOLATION RELAYS**

RETURN

Ends a subroutine and returns operation to the line after the last executed GOSUB command.

<CR>

Carriage return character, decimal 13.

<LF>

Line feed character, decimal 10.

## Programming Examples In BASIC

The following sample BASIC programs show how commands for the VX4730 might be used. These examples assume that the VX4730 has logical address 2 and is installed in a VXIbus mainframe that is controlled via an IEEE-488 interface from an external system controller, such as an IBM PC or equivalent, using a National Instruments IEEE-488 interface. The VXIbus IEEE-488 interface is assumed to have an IEEE-488 primary address of decimal 24 and to have converted the VX4730 Module's logical address to an IEEE-488 primary address of decimal 2.

The command sequence terminator character <TM> used in the example programs is a line feed character, which is appended to output data strings using the BASIC command CHR$(10). That is, DATA# = "....." +CHR$(10).

Following each example, the data sent to and returned from the module is shown, with data returned by the module shown <u>underlined</u>.

<u>Example 1</u>:

```
10  '****************** VX4730 BASIC EXAMPLE PROGRAM *******************
20  '
30  '           USING NATIONAL INSTRUMENT PCIIA CALLS
40  '           ASSUMES VX4730 GPIB ADDRESS = 2
50  '
100 ' ****************** INITIALIZE SYSTEM ***************************
110  CLEAR , 60000!: IBINIT1 = 60000!: IBINIT2 = IBINIT1 + 3: BLOAD "bib.m", IBINIT1
120  CALL IBINIT1(IBFIND, IBTRG, IBCLR, IBPCT, IBSIC, IBLOC, IBPPC, IBBNA, IBONL, IBRSC,
     IBSRE, IBRSV, IBPAD, IBSAD, IBIST, IBDMA, IBEOS, IBTMO, IBEOT, IBRDF, IBWRTF, IBTRAP)
```

```
130 CALL IBINIT2(IBGTS, IBCAC, IBWAIT, IBPOKE, IBWRT, IBWRTA, IBCMD, IBCMDA, IBRD,
    IBRDA, IBSTOP, IBRPP, IBRSP, IBDIAG, IBXTRC, IBRDI, IBWRTI, IBRDIA, IBWRTIA, IBSTA%,
    IBERR%, IBCNT%)
140 CLS : BDNAME$ = "PCX"
150 CALL IBFIND(BDNAME$, PCX%)
160 IF PCX% < 0 THEN PRINT "IEEE FAILED": END
170 '
200 '******************** DISPLAY VXI TABLE **************************
210 DEVADDR% = 1                    'ADDRESS OF RESOURCE MANAGER
220 CALL IBPAD(PCX%, DEVADDR%)      'ASSIGN DEVICE ADDRESS TO GPIB
230 TM$ = CHR$(13) + CHR$(10)       'DEFINE LINE TERMINATOR MESSAGE
240 WRT$ = "TABLE" + TM$
250 CALL IBWRT(PCX%, WRT$)          'WRITE TABLE COMMAND TO RESOURCE MANAGER
260 CLS
270 PRINT "The VXI system contains the following Modules. "
280 PRINT "***********************************************************"
290 FOR I = 1 TO 6              'ASSUMES 5 INSTRUMENTS + RESOURCE MANAGER
300 RD$ = SPACE$(250)           'ASSIGN SPACE FOR READ STRING
310 CALL IBRD(PCX%, RD$)        'CALL READ FUNCTION
320 PRINT LEFT$(RD$, IBCNT%);   'DISPLAY RESPONSE
330 NEXT I
340 PRINT "PRESS ENTER TO CONTINUE"  'PAUSE PROGRAM
350 INPUT A$
360 '
400 '**************** CONNECT A AND B CHANNEL DAC'S OUTPUTS **************
410 '                 TO THE MODULE'S OUTPUT CONNECTOR
420 CLS
430 DEVADDR% = 2                    'ASSUMES VX4730 GPIB ADDRESS = 2
440 CALL IBPAD(PCX%, DEVADDR%)      'ASSIGN DEVICE ADDRESS TO GPIB
450 WRT$ = "CLS A,B" + TM$          'COMMAND TO CONNECT A & B DAC OUTPUTS
460 CALL IBWRT(PCX%, WRT$)          'SEND COMMAND TO VX4730
470 '
500 '***** PROGRAM VX4730 OUTPUTS A & B FOR 10.0 & 5.00 VOLTS RESPECTIVELY ****
510 CLS
520 PRINT "CHANNEL A = 10.0 VOLTS DC" + TM$
530 PRINT "CHANNEL B = 5.00 VOLTS DC" + TM$
540 '
550 WRT$ = "VA 10;VB 5.00" + TM$   'COMMAND TO PROGRAM OUTPUT VOLTAGE OF
DAC'S
560 CALL IBWRT(PCX%, WRT$)          'SEND COMMAND TO MODULE
570 END
```

The commands and data sent to the VX4730 Module are:

```
CLS A,B<LF>
VA 10;VB 5.00<LF>
```

Example 2:

```
10 '****************** VX4730 BASIC EXAMPLE PROGRAM ******************
20 '
30 '         USING NATIONAL INSTRUMENT PCIIA CALLS
40 '         ASSUMES VX4730 GPIB ADDRESS = 2
50 '
100 ' ***************** INITIALIZE SYSTEM ***************************
110  CLEAR , 60000!: IBINIT1 = 60000!: IBINIT2 = IBINIT1 + 3: BLOAD "bib.m", IBINIT1
120  CALL IBINIT1(IBFIND, IBTRG, IBCLR, IBPCT, IBSIC, IBLOC, IBPPC, IBBNA, IBONL, IBRSC,
     IBSRE, IBRSV, IBPAD, IBSAD, IBIST, IBDMA, IBEOS, IBTMO, IBEOT, IBRDF, IBWRTF,
     IBTRAP)
130  CALL IBINIT2(IBGTS, IBCAC, IBWAIT, IBPOKE, IBWRT, IBWRTA, IBCMD, IBCMDA, IBRD,
     IBRDA, IBSTOP, IBRPP, IBRSP, IBDIAG, IBXTRC, IBRDI, IBWRTI, IBRDIA, IBWRTIA, IBSTA%,
     IBERR%, IBCNT%)
140 CLS : BDNAME$ = "PCX"
150 CALL IBFIND(BDNAME$, PCX%)
160 IF PCX% < 0 THEN PRINT "IEEE FAILED": END
170 RD$ = SPACE$(80)
180 '
200 '****************** INITIATE VX4730 SELF TEST *****************
210 CLS
220 DEVADDR% = 2                'ASSUMES VX4730 GPIB ADDRESS = 2
230 CALL IBPAD(PCX%, DEVADDR%)  'ASSIGN DEVICE ADDRESS TO GPIB
240 WRT$ = "RST" + TM$          'RESET CARD TO POWER UP STATE
250 CALL IBWRT(PCX%, WRT$)      'SEND RESET COMMAND TO VX4750
260 WRT$ = "IST" + TM$          'INITIATE SELF TEST
270 CALL IBWRT(PCX%, WRT$)      'SEND SELF TEST TO VX4730
300 '************** CHECK VX4730 FOR ANY ERRORS ***************************
    'CALL READ FUNCTION
310 PRINT "TESTING VX4730 FOR ERRORS >" + TM$
320 GOSUB 500                         'READ AND DISPLAY VX4730 STATUS
330 PRINT "PRESS ENTER TO END PROGRAM" 'PAUSE PROGRAM
340 INPUT A$
350 '
400 END
500 '****************** READ BACK VX4730 STATUS **********************
510 PRINT "       * * VX4730 STATUS * *" + TM$
520 WRT$ = "ERR?" + TM$               'MODULE ERROR INQUIRY COMMAND
530 CALL IBWRT(PCX%, WRT$)            'SEND COMMAND TO VX4730
540 CALL IBRD(PCX%, RD$)              'CALL READ FUNCTION
550 PRINT "     "; LEFT$(RD$, IBCNT%) 'DISPLAY RESPONSE
560 PRINT
570 IF MID$(RD$, 1, 1) = "0" THEN GOTO 600 'TEST FOR MORE ERRORS IN QUE
580 GOTO 540                          'REPEAT READING IF MORE ERRORS
590 PRINT
600 RETURN
```

The commands and data sent to the VX4730 Module and the response data returned are shown below. Response data is underlined.

```
IST<LF>
ERR?<LF>
0,0,NO ADDITIONAL ERRORS TO REPORT<CR><LF>
```

# Appendix A
# VXIbus Operation

CAUTION

*If the user's mainframe has other manufacturer's computer boards operating in the role of VXIbus foreign devices, the assertion of BERR* (as defined by the VXIbus Specification) may cause operating problems on these boards.*

The VX4730 Module is a C size single slot VXIbus Message-Based Word Serial instrument. It uses the A16, D16 VME interface available on the backplane P1 connector and does not require any A24 or A32 address space. The module is a D16 interrupter.

The VX4730 Module is neither a VXIbus commander nor a VMEbus master, and therefore it does not have a VXIbus signal register. The VX4730 is a VXIbus message based servant.

The module supports both the Normal Transfer mode and Fast Handshake Transfer mode of the VXIbus, using the Write Ready and Read Ready bits of the module's Response register.

A Normal Transfer mode Read of the VX4730 Module proceeds as follows:

1. The commander reads the VX4730's Response register and checks if the Write Ready and DOR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll these bits until they become true.

2. The commander writes the Byte Request command (0DEFFh) to the VX4286's Data Low register.

3. The commander reads the VX4730's Response register and checks if the Read Ready and DOR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll these bits until they become true.

4. The commander reads the VX4730's Data Low register.

A Normal Transfer Mode Write to the VX4730 Module proceeds as follows:

1. The commander reads the VX4730's Response register and checks if the Write Ready and DIR bits are true. If they are, the commander proceeds to the next

step. If not, the commander continues to poll the Write Ready and DIR bits until they are true.

2. The commander writes the Byte Available command which contains the data (0BCXX or 0BDXX, depending on the End bit) to the VX4730's Data Low register.

The VX4730 Module also supports the Fast Handshake mode during some commands. In this mode, data typically can be sent at a 400 Kbyte rate. The VX4730 Module asserts BERR* to switch from Fast Handshake Mode back to Normal Transfer mode, per VXI Specification. The VX4730's Read Ready and Write Ready bits react properly during Fast Handshake.

A Fast Handshake Transfer Mode Read of the VX4730 Module proceeds as follows:

1. The commander writes the Byte Request command (0DEFFh) to the VX4730's Data Low register.

2. The commander reads the VX4730's Data Low register.

A Fast Handshake Transfer Mode Write to the VX4730 Module proceeds as follows:

1. The commander writes the Byte Available command which contains the data (0BCXX or 0BDXX depending on the state of the End bit) to the VX4730's Data Low register.

The VX4730 Module has no registers beyond those defined for VXIbus message based devices. All communications with the module are through the data low register, the response register or the VXIbus interrupt cycle.

As with all VXIbus devices, the VX4730 Module has registers located within a 64 byte block in the A16 address space. The base address of the VX4730 device's registers is determined by the device's unique logical address and can be calculated as follows:

Base Address = V * 40H + C000H

where V is the device's logical address as set in the logical address switches.

## VX4730 Configuration Registers

Below is a list of the VX4730 Configuration Registers with a complete description of each. In this list, RO = Read Only, WO = Write Only, R = Read, and W = Write. The offset is relative to the module's base address. An 'x' in a Value bit position in the Bit Definition table means that either a 0 or 1 is acceptable in that position.

## REGISTER DEFINITIONS

| Register | Address | Type | Value (Bits 15-0) |
|---|---|---|---|
| ID Register | 0000H | RO | 1011 1111 1111 1100 (BFFCh) |
| Device Type | 0002H | RO | See Device Type definition below |
| Status | 0004H | R | See Device Type definition below |
| Control | 0004H | W | See Device Type definition below |
| Offset | 0006H | WO | Not used |
| Protocol | 0008H | RO | 1111 1110 1111 1111 (F7FFh) |
| Response | 000AH | RO | Defined by state of the interface |
| Data High | 000CH | | Not used |
| Data Low | 000EH | W | See Data Low definition below |
| Data Low | 000EH | R | See Data Low definition below |

## REGISTER BIT DEFINITIONS

| | |
|---|---|
| ID: | BFFCh |
| Device: | F525h |
| Protocol: | F7FFh |

### Word Serial Commands

A write to the Data Low register causes this module to execute some action based on the data written. This section describes the device-specific Word Serial commands this module responds to and the results of these commands.

Read Protocol command response: FE6Bh

# Appendix B
# Input/Output Connections

All DAC outputs are provided on four DE-9S connectors, labeled S1 through S4. These connectors may be accessed using either Tektronix/CDS VX1732 Analog Cables or VX1784P Hooded Connectors.

S1

| Pin number | Signal |
|---|---|
| 1 | Front Panel Ground (for Cable Shield) |
| 2 | D/A channel C signal |
| 3 | D/A channel B signal |
| 4 | D/A channel A signal |
| 5 | Unused |
| 6 | D/A channel C return |
| 7 | D/A channel B return |
| 8 | D/A channel A return |
| 9 | Ground |

S2

| Pin number | Signal |
|---|---|
| 1 | Front Panel Ground (for Cable Shield) |
| 2 | D/A channel F signal |
| 3 | D/A channel E signal |
| 4 | D/A channel D signal |
| 5 | Unused |
| 6 | D/A channel F return |
| 7 | D/A channel E return |
| 8 | D/A channel D return |
| 9 | Ground |

S3

| Pin number | Signal |
|---|---|
| 1 | Front Panel Ground (for Cable Shield) |
| 2 | D/A channel I signal |
| 3 | D/A channel H signal |
| 4 | D/A channel G signal |
| 5 | Unused |
| 6 | D/A channel I return |
| 7 | D/A channel H return |
| 8 | D/A channel G return |
| 9 | Ground |

S4

| Pin number | Signal |
|---|---|
| 1 | Front Panel Ground (for Cable Shield) |
| 2 | D/A channel L signal |
| 3 | D/A channel K signal |
| 4 | D/A channel J signal |
| 5 | Unused |
| 6 | D/A channel L return |
| 7 | D/A channel K return |
| 8 | D/A channel J return |
| 9 | Ground |

# Appendix C
# VXI Glossary

The terms in this glossary are defined as used in the VXIbus System. Although some of these terms may have different meanings in other systems, it is important to use these definitions in VXIbus applications. Terms which apply only to a particular instrument module are noted. Not all terms appear in every manual.

**Term** **Definition**

**Accessed Indicator** An amber LED indicator that lights when the module identity is selected by the Resource Manager module, and flashes during any I/O operation for the module.

**ACFAIL*** A VMEbus backplane line that is asserted under these conditions: 1) by the mainframe Power Supply when a power failure has occurred (either ac line source or power supply malfunction), or 2) by the front panel ON/STANDBY switch when switched to STANDBY.

**A-Size Card** A VXIbus instrument module that is 100.0 by 160 mm by 20.32 mm (3.9 by 6.3 in by 0.8 in), the same size as a VMEbus single-height short module.

**Asynchronous Communication** Communications that occur outside the normal "command-response" cycle. Such communications have higher priority than synchronous communication.

**Backplane** The printed circuit board that is mounted in a VXIbus mainframe to provide the interface between VXIbus modules and between those modules and the external system.

**B-Size Card** A VXIbus instrument module that is 233.4 by 160 mm by 20.32 mm (9.2 by 6.3 in by 0.8 in), the same size as a VMEbus double-height short module.

**Bus Arbitration** In the VMEbus interface, a system for resolving contention for service among VMEbus Master devices on the VMEbus.

**Bus Timer** A functional module that measures the duration of each data transfer on the Data Transfer Bus (DTB) and terminates the DTB cycle if the duration is excessive. Without the termination capability of this module, a Bus Master attempt to transfer data to or from a non-existent Slave location could result in an infinitely long wait for the Slave response.

**Client** In shared memory protocol (SMP), that half of an SMP channel that does not control the shared memory buffers.

**CLK10** A 10 MHz, ±100 ppm, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1-12 on P2. It is distributed to each module slot as a single source, single destination signal with a matched delay of under 8 ns.

**CLK100** A 100 MHz, ±100 ppm, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1-12 on P3. It is distributed to each module slot in synchronous with CLK10 as a single source, single destination signal with a maximum system timing skew of 2 ns, and a maximum total delay of 8 ns.

**Commander** In the VXIbus interface, a device that controls another device (a servant). A commander may be a servant of another commander.

**Command** A directive to a device. There are three types of commands:

In Word Serial Protocol, a 16-bit imperative to a servant from its commander.

In Shared Memory Protocol, a 16-bit imperative from a client to a server, or vice versa.

In a Message, an ASCII-coded, multi-byte directive to any receiving device.

**Communication Registers** In word serial protocol, a set of device registers that are accessible to the commander of the device. Such registers are used for inter-device communications, and are required on all VXIbus message-based devices.

**Configuration Registers** A set of registers that allow the system to identify a (module) device type, model, manufacturer, address space, and memory requirements. In order to support automatic system and memory configuration, the VXIbus standard specifies that all VXIbus devices have a set of such registers, all accessible from P1 on the VMEbus.

**C-Size Card** A VXIbus instrument module that is 340.0 by 233.4 mm by 30.48 mm (13.4 by 9.2 in by 1.2 in).

**Custom Device** A special-purpose VXIbus device that has configuration registers so as to be identified by the system and to allow for definition of future device types to support further levels of compatibility.

**Data Transfer Bus** One of four buses on the VMEbus backplane. The Data Transfer Bus allows Bus Masters to direct the transfer of binary data between Masters and Slaves.

**DC SUPPLIES Indicator** A red LED indicator that illuminates when a DC power fault is detected on the backplane.

**Device Specific Protocol** A protocol for communication with a device that is not defined in the VXIbus specification.

**D-Size Card** A VXIbus instrument module that is 340.0 by 366.7 mm by 30.48 mm (13.4 x 14.4 in x 1.2 in).

**DTB** See Data Transfer Bus.

**DTB Arbiter** A functional module that accepts bus requests from Requester modules and grants control of the DTB to one Requester at a time.

**DUT** Device Under Test.

**ECLTRG** Six single-ended ECL trigger lines (two on P2 and four on P3) that function as inter-module timing resources, and that are bussed across the VXIbus subsystem backplane. Any module, including the Slot 0 module, may drive and receive information from these lines. These lines have an impedance of 50 ohms; the asserted state is logical High.

**Embedded Address** An address in a communications protocol in which the destination of the message is included in the message.

**ESTST** Extended STart/STop protocol; used to synchronize VXIbus modules.

**Extended Self Test** Any self test or diagnostic power-up routine that executes after the initial kernel self test program.

**External System Controller** The host computer or other external controller that exerts overall control over VXIbus operations.

**FAILED Indicator** A red LED indicator that lights when a device on the VXIbus has detected an internal fault. This might result in the assertion of the SYSFAIL* line.

**IACK Daisy Chain Driver** The circuit that drives the VMEbus Interrupt Acknowledge daisy chain line that runs continuously through all installed modules or through jumpers across the backplane.

**ID-ROM** An NVRAM storage area that provides for non-volatile storage of diagnostic data.

**Instrument Module** A plug-in printed circuit board, with associated components and shields, that may be installed in a VXIbus mainframe. An instrument module may contain more than one device. Also, one device may require more than one instrument module.

**Interface Device** A VXIbus device that provides one or more interfaces to external equipment.

**Interrupt Handler** A functional module that detects interrupt requests generated by Interrupters and responds to those requests by requesting status and identity information.

**Interrupter** A device capable of asserting VMEbus interrupts and performing the interrupt acknowledge sequence.

**IRQ** The Interrupt ReQuest signal, which is the VMEbus interrupt line that is asserted by an Interrupter to signify to the controller that a device on the bus requires service by the controller.

**Local Bus** A daisy-chained bus that connects adjacent VXIbus slots.

**Local Controller** The instrument module that performs system control and external interface functions for the instrument modules in a VXIbus mainframe or several mainframes. See Resource Manager.

**Local Processor** The processor on an instrument module.

**Logical Address** The smallest functional unit recognized by a VXIbus system. It is often used to identify a particular module.

**Mainframe** **Card Cage** For example, the Tektronix VX1400 Mainframe, an operable housing that includes 13 C-size VXIbus instrument module slots.

**Memory Device** A storage element (such as bubble memory, RAM, and ROM) that has configuration registers and memory attributes (such as type and access time).

**Message** A series of data bytes that are treated as a single communication, with a well defined terminator and message body.

**Message Based Device** A VXIbus device that supports VXI configuration and communication registers. Such devices support the word serial protocol, and possibly other message-based protocols.

**MODID Lines** Module/system identity lines.

**Physical Address** The address assigned to a backplane slot during an access.

**Power Monitor** A device that monitors backplane power and reports fault conditions.

**P1** The top-most backplane connector for a given module slot in a vertical mainframe such as the Tektronix VX1400. The left-most backplane connector for a given slot in a horizontal mainframe.

**P2** The bottom backplane connector for a given module slot in a vertical C-size mainframe such as the VX1400; or the middle backplane connector for a given module slot in a vertical D-size mainframe such as the VX1500.

**P3** The bottom backplane connector for a given module slot in a vertical D-size mainframe such as the Tektronix VX1500.

**Query** A form of command that allows for inquiry to obtain status or data.

**READY Indicator** A green LED indicator that lights when the power-up diagnostic routines have been completed successfully. An internal failure or failure of +5-volt power will extinguish this indicator.

**Register Based Device** A VXIbus device that supports VXI register maps, but not high level VXIbus communication protocols; includes devices that are register-based servant elements.

**Requester** A functional module that resides on the same module as a Master or Interrupt Handler and requests use of the DTB whenever its Master or Interrupt Handler requires it.

**Resource Manager** A VXIbus device that provides configuration management services such as address map configuration, determining system hierarchy, allocating shared system resources, performing system self test diagnostics, and initializing system commanders.

**Self Calibration** A routine that verifies the basic calibration of the instrument module circuits, and adjusts this calibration to compensate for short- and long-term variables.

**Self Test** A set of routines that determine if the instrument module circuits will perform according to a given set of standards. A self test routine is performed upon power-up.

**Servant** A VXIbus message-based device that is controlled by a commander.

**Server** A shared memory device that controls the shared memory buffers used in a given Shared Memory Protocol channel.

**Shared Memory Protocol** A communications protocol that uses a block of memory that is accessible to both client and server. The memory block operates as a message buffer for communications.

**Slot 0 Controller** See Slot 0 Module. Also see Resource Manager.

**Slot 0 Module** A VXIbus device that provides the minimum VXIbus slot 0 services to slots 1 through 12 (CLK10 and the module identity lines), but that may provide other services such as CLK100, SYNC100, STARBUS, and trigger control.

**SMP** See Shared Memory Protocol.

**STARX** Two (2) bi-directional, 50 ohm, differential ECL lines that provide for inter-module asynchronous communication. These pairs of timed and matched delay lines connect slot 0 and each of slots 1 through 12 in a mainframe. The delay between slots is less than 5 nanoseconds, and the lines are well matched for timing skew.

**STARY** Two (2) bi-directional, 50 ohm, differential ECL lines that provide for inter-module asynchronous communication. These pairs of timed and matched delay lines connect slot 0 and each of slots 1 through 12 in a mainframe. The delay between slots is less than 5 nanoseconds, and the lines are well matched for timing skew.

**STST** STart/STop protocol; used to synchronize modules.

**SYNC100** A Slot 0 signal that is used to synchronize multiple devices with respect to a given rising edge of CLK100. These signals are individually buffered and matched to less than 2ns of skew.

**Synchronous Communications** A communications system that follows the "command-response" cycle model. In this model, a device issues a command to another device; the second device executes the command; then returns a response. Synchronous commands are executed in the order received.

**SYSFAIL*** A signal line on the VMEbus that is used to indicate a failure by a device. The device that fails asserts this line.

**System Clock Driver** A functional module that provides a 16-MHz timing signal on the Utility Bus.

**System Hierarchy** The tree structure of the commander/servant relationships of all devices in the system at a given time. In the VXIbus structure, each servant has a commander. A commander may also have a commander.

**Test Monitor** An executive routine that is responsible for executing the self tests, storing any errors in the ID-ROM, and reporting such errors to the Resource Manager.

**Test Program** A program, executed on the system controller, that controls the execution of tests within the test system.

**Test System** A collection of hardware and software modules that operate in concert to test a target DUT.

**TTLTRG** Open collector TTL lines used for inter-module timing and communication.

**VXIbus Subsystem** One mainframe with modules installed. The installed modules include one module that performs slot 0 functions and a given complement of instrument modules. The subsystem may also include a Resource Manager.

**Word Serial Protocol** A VXIbus word oriented, bi-directional, serial protocol for communications between message-based devices (that is, devices that include communication registers in addition to configuration registers).

**Word Serial Communications** Inter-device communications using the Word Serial Protocol.

**WSP** See Word Serial Protocol.

**10-MHz Clock** A 10 MHz, ±100 ppm timing reference. Also see CLK10.

**100-MHz Clock** A 100 MHz, ±100 ppm clock synchronized with CLK10. Also see CLK100.

**488-To-VXIbus Interface** A message based device that provides for communication between the IEEE-488 bus and VXIbus instrument modules.

# Appendix D
# Calculating Module Current

The VX4730 DAC Module supplies voltage and current to an external load. It is necessary to calculate the amount of current that is drawn by each load in order to determine the number of channels that may be used on a single VX4730 or the number of VX4730 Modules that may be used in a mainframe.

For each channel used, calculate the maximum current drawn. Typically, this is the maximum voltage to be programmed divided by the load impedance. Add up all the currents of all the channels to be used. The total must not exceed 720 milliamps and no one channel can exceed 410 milliamps. If the total does exceed 720 milliamps, a second VX4730 is needed. Repeat this process until all of the system requirements are met without exceeding the VX4730's maximum current specification.

The next step is to determine if the mainframe being used has enough current capacity on the ±24 volt rails to support the number of VX4730's being used as well as any other module(s) that uses ±24 volts. The total ±24 volt current needs of the VX4730 are the calculated load current plus 480 milliamps. Therefore, if a module is using the full 720 milliamp capacity, the total for the VX4730 will be 1.2 amps.

The mainframe being used will specify the capacity of its ±24 volt power supply. This is 6 amps on both the +24V and the -24V supply rails if a Tektronix/CDS VX1401 Mainframe is being used. The VX1401 can accommodate five fully loaded VX4730 modules. The VX1400 Mainframe can supply 8 amps on both the +24V and -24V supply rails, which allows the possibility of using six fully loaded VX4730 Modules.

# Appendix M
# MATE Programming

This Appendix defines the programming commands to be used with the VX4730 when the module has been ordered with Option 1M. With Option 1M installed, the VX4730 includes an embedded CCI (CIIL Communications Interface) that fulfills the United States Air Force MATE system IAC (Instrument-on-A-Card) requirements for isolated self test and remote programming via MATE CIIL (Control Interface Intermediate Language) commands. This allows the VX4730 to be programmed as a DC Supply (DCS).

The following subjects are covered in this manual section:

The user is assumed to be familiar with the ATLAS (Abbreviated Test Language for All Systems) programming language as it is applied to MATE systems.

## CIIL / Commercial Differences

The CIIL implementation of this module differs from operations described in the body of this manual in some respects.

CIIL does not allow interrupts to be enabled for IEEE-488 Service Requests. It always operates in the nonbuffered mode, and supports the standard CIIL commands and data syntax, which excludes the binary data syntax.

Because the self test takes under five seconds, the confidence and self test are identical on this module.

The following specifications differ with the CIIL option installed:

VXI Data Rate:
    400 bytes/sec minimum

VXIbus Protocol Events Supported:
    VXIbus events are returned by this module via VME interrupts. This module supports the following event:

    UNRECOGNIZED COMMAND

Conversion Rate:

Throughput is the maximum number of conversions per second which can be accomplished by the DAC on a continuous basis. This module is capable of a conversion rate in excess of 500 conversions per second per channel.

CIIL Command Mnemonics and Definitions

The VX4730 Module is controlled by CIIL commands issued to the module by the module's VXIbus commander over the VXIbus mainframe backplane. The module's commander is interfaced to the MATE station computer via an IEEE-488 interface bus. A typical control sequence for the module is as follows:

1) Set up the voltage output of a given channel.

2) Connect the output pins of the module to the UUT (Unit Under Test) via the MATE ICA (Interface Control Assembly).

3) Close the channel's isolation relay, connecting the channel's voltage output to the VX4730's front panel connector.

4) Open the channel's isolation relay, disconnecting the channel's output from the module's front panel connector.

Each CIIL command consists of a verb and up to three different types of operands. The operands are nouns, modifiers, and modifier values. Depending on the verb, a given operand may or may not be required.

If the module detects syntax errors in a transmission, the entire transmission and all future transmissions are ignored until a STA (Status) command is received. Following a STA command, the station computer requests input from the module and receives an ASCII message, identifying the module status as error or no error.

Verbs

| Mnemonic | Definition |
|---|---|
| CIIL | Return from alternate language: This command should be sent to return to the CIIL environment after a GAL instruction. Any pending errors are discarded, request true interrupts are disabled, and buffered mode is terminated if previously entered while in the alternate language. |
| CLS | Close: commands the module to close the specified isolation relay. |
| CNF | Confidence Test: commands the module to perform a confidence test. An error message is queued if hardware malfunctions are encountered during the test. The queued error message is returned to the station computer when the module receives an STA command. The confidence test takes less than five seconds to execute. The test performed is described under the IST command in the Operation section of this manual. The same test is performed for both the CIIL CNF and IST commands. |

FNC Function: identifies a channel to be set up and indicates the start of a setup sequence.

GAL Go to Alternate Language: Allows any command listed in the Operation section of this manual to be executed. Any pending errors are discarded before going to the alternate language.

IST Internal Self Test: commands the module to perform a self test. An error message is queued if hardware malfunctions are encountered during the self test. The queued error message is returned to the station computer when the module receives an STA command. The internal self test takes less than 5 seconds to execute. The test performed is described under the IST command in the Operations Section of this manual. The same test is performed for both the CIIL CNF and IST commands.

OPN Open: commands the module to open a specified channel's isolation relay.

RST Reset: Opens the specified channel's isolation relay and sets its output voltage to 0.000 volts.

SET Setup: used to indicate the beginning of the set-up of a module DAC channel.

SID Self Identification: commands the module to return an identification string in the following format:

<SP>COLORADO DATA SYSTEMS;VX4730;0;<REV>; <STATUS RESPONSE><CR><LF>

where:
<SP> = space
<CR> = carriage return
<LF> = line feed
<REV> = revision level (e.g. 1.0)
<STATUS RESPONSE> = the ASCII message that would normally be returned in response to a STA command, in accordance with MATE-STD-2806763, paragraphs 5.3.4 and 5.3.4.2.

STA Status: commands the module to report its current status and/or any error that has been queued to the station computer.

Nouns

DCS DC Source: the CIIL noun defining the general class of this module's output.

Modifiers

VOLT Voltage: indicates the programmable parameter to be set.

## CIIL Command Structures and Formats

This sub-section defines the ordering of commands that are accepted by this module. Except for the FNC command, each command is transmitted separately and terminated with a <CR><LF>. The FNC command appears as the first command in a sequence, followed by all other commands (ie: SET) in the same transmission. One <CR><LF> is sent at the end of the transmission. The symbols used in the syntax expansions are defined below.

## Symbol Definition

< > Item referenced later (enclosed between symbols)

[ ] Optional item or structure (enclosed between symbols)

"---" No operand required or expected

"y" Decimal value is in signed scientific notation with no embedded blanks (sign may be + or - ; no sign means +). The mantissa is 10 characters; the exponent is two characters with a mandatory sign. All numbers are rounded to the nearest half millivolt. Valid syntaxes are:

```
+.9000000000E+01
+.2559000000E+01
+.2559400000E+01 (rounded to +2.5595 volts)
```

The values may be programmed from -16.3835 to +16.3835 volts for each channel. See the V and S commands in the Operation section of this manual.

z 1-2 digit integer value. For this module, the acceptable values are 0 through 11, representing channels A through L, respectively.

## CIIL Syntax Expansions

<voltage value set up> :: [FNC DCS :CH<z> SET VOLT<y><CR><LF>]

<channel isolation relay-close> :: [CLS :CH<z><CR><LF>]

<channel isolation relay-open> :: [OPN :CH<z><CR><LF>]

<module self test> :: [IST<CR><LF>]

<module confidence test> :: [CNF<CR><LF>]

<reset channel to default value> :: [RST DCS :CH<z><CR><LF>]

<request status read back> :: [STA<CR><LF>]

<module normal response to STA> :: ASCII SPACE<CR><LF>

<module abnormal response to STA> :: [F07DCS (MOD): <error description><CR><LF>]

<chan-val>, where used in error descriptions, is 0 through 11, specifying the channel (A through L).

The following error descriptions are supported:

SELF TEST FAILURE: BAD VOLTAGE CHAN <chan-val>,...<chan-val><CR><LF>

The output voltage changed during self test but was not within 3% or 0.5 volts of the required value.

VOLTAGE OVERRANGE CHAN <chan-val><CR><LF>

The data value sent in conjunction with the VOLT command was out of range. This error occurs if the programmed voltage value is greater or equal to +16.38375.

VOLTAGE UNDERRANGE CHAN <chan-val><CR><LF>

The data value sent in conjunction with the VOLT command was out of range. This error occurs if the programmed voltage value is less than or equal to -16.38375.

RELAY STAYS IN CLOSED POSITION CHAN <chan-val><CR><LF>

This error occurs when an isolation relay stays in the closed position after receiving an OPN command.

RELAY STAYS IN OPEN POSITION CHAN <chan-val><CR><LF>

This error occurs when an isolation relay stays in the OPEN position after receiving a CLS command.

RECEIVED UNEXPECTED [CHR] WHILE [REASON]<CR><LF>

For this response:

[CHR] = [single quote][character][single quote] for printable characters (20 hex through 7F hex), for example, 'G'.
or
[CHR] = [space][hex digit][hex digit] for nonprintable characters (00 hex through 19 hex and 80 hex through FF hex), for example, 0A .

<REASON> = ONE OF THE FOLLOWING:
- PARSING CHANNEL.
- EXPECTING A LINE FEED.
- EXPECTING A VOLTAGE.
- PARSING MANTISSA.
- PARSING EXPONENT.

ILLEGAL CHANNEL<chan><CR><LF>

Incorrect channel number received. <chan> is the incorrect channel number received, two digits maximum.

SET VOLTAGE COMMAND WITH VOLTAGE OMITTED<CR><LF>

Channel specified without corresponding voltage.

TOO MANY DIGITS IN EXPONENT<CR><LF>

Exponent of voltage value exceeds three digits.

UNRECOGNIZED COMMAND<CR><LF>

This error occurs if a command that is not a valid CIIL command is received by the module.

ATLAS and CIIL Syntax

This sub-section provides examples of the ATLAS syntax that can be used to control the module. The ATLAS syntax is shown, followed by the corresponding CIIL command expansions. The symbol definitions used in the syntax expansions are as follows:

| Symbol | Definition |
|---|---|
| < > | Item reference defined later (enclosed between symbols) |
| [ ] | Optional item or structure (enclosed between symbols) |
| :: | Is defined to be |
| { } | Set of choices or boundaries of a structure of inseparable items (enclosed between symbols) |
| : | Exclusive OR |
| ... | Optional repetition |

| Term | Definition |
|---|---|
| <integer-val> | Integer |
| <integer-list> | A list of integers |
| <real-val> | Decimal number |
| <real-list> | A list of decimal numbers |
| <connection> | Connection field as defined in ATLAS program. |
| <chan-num> | Channel number |
| <statno> | Statement number |
| <CR> | Carriage return |
| <LF> | Line feed |
| <SP> | Space |
| <units> | Units of measure of specified value. |

*NOTE*: <chan-num> is an integer from 0 through 11 allocated by the ATLAS compiler during its allocate phase, derived from the connection field of the ATLAS statement. The <chan-num> directly corresponds to DAC channels A through L respectively.

Examples:

The examples that follow use single-action verbs. It is also possible to use multi-action verbs which will issue combinations of CIIL strings for each ATLAS statement. For further details, consult the ATLAS Compiler manual.

Set up a voltage output value.

<statno> SETUP,DC SIGNAL, VOLTAGE <real-val> <units>, CNX <connect field> $

CIIL Expansion

FNC DCS :CH<chan-num> SET VOLT <real-val><CR><LF>

Connect the output pins of the module to the UUT (Unit Under Test) via the MATE ICA.

<statno> CONNECT,DC SIGNAL, VOLTAGE <real-val> <units>, CNX <connection field> $

CIIL Expansion

CON <connection data><CR><LF>

The above CIIL message is sent to the MATE ICA and not to the module.

Connect the output pins of the module to the UUT (Unit Under Test) via the MATE ICA.

<statno> CLOSE,DC SIGNAL, VOLTAGE <real-val> <units>, CNX <connection field> $
CIIL Expansion

CLS :CH<chan-num><CR><LF>

Open the channel's isolation relay, disconnecting the channel's output from the module's front panel connector.

<statno> OPEN,DC SIGNAL, VOLTAGE <real-val> <units>, CNX <connection field> $

CIIL Expansions

OPN :CH<chan-num><CR><LF>